A Power-Efficient LC Quadrature VCO for RFID, Zigbee and Bluetooth Standards

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***Abstract*—A multi-band CMOS LC Quadrature Voltage Control Oscillator (QVCO) with minimum power consumption is developed to meet the phase noise and frequency band requirements of RFID, Zigbee and Bluetooth standards. To accomplish the multi-band receiving architecture at low power consumption, current switching technique with optimized cross-coupled transistor sizes has been used. A comprehensive analysis of small signal model for complementary architecture including transistor noise sources and their effects on output phase noise amount has been discussed. Using extracted small signal model, coupled and coupling transistor sizes for minimum power consumption and the least achievable phase noise have been optimized. Designed QVCO has been implemented using TSMC 0.18um CMOS technology operating at 1.8V supply voltage. Proposed QVCO generates two separated frequency bands of 1.65-1.85GHz and 2.4-2.5GHz with phase noise of -125dBc/Hz at frequency offset of 3MHz. The total current drawn by QVCO is 7.5mA which makes the power consumption as low as 13.5mW.**

***Index Terms*—Power Efficient, Quadrature Voltage Control Oscillator, Zigbee Standard, Bluetooth standard, RFID**

I. INTRODUCTION

The voltage-controlled oscillator (VCO) is an essential building block of a wireless communication system used in frequency synthesizers. According to commonly-used standards, RFID (EPC-Global Gen II) RF frequency band is 902-928MHz (and 860-960MHz) while Zigbee (IEEE 802.15.4) works in two frequency bands of 828-928MHz and 2.4-2.5GHz with frequency modulation of BPSK and QPSK respectively. Required phase noise at frequency offset of 3MHz is -100dBc/Hz for QPSK modulation state. Bluetooth standard frequency band is the same with Zigbee with phase noise of -120dBc/Hz at frequency offset of 3MHz [1-3]. To realize these standards in an integrated hardware platform effectively, the RF front-end module need be well addressed [4]. Moreover, the integrated QVCO can produce quadrature signal at different frequency bands using a common circuit block with minimized overhead to support multi-standards. Producing quadrature signal for Zigbee standard with required phase noise of Bluetooth with the minimum power consumption will be a hard work. Recently, a CMOS VCO could be implemented using a ring structure or an LC tank. A ring VCO has the benefit of a wide tuning range and the drawback of a high phase noise making it disqualified for most structures in modern RF transceivers. However, novel ring based wide range VCOs with acceptable phase noise have been presented [5], but they suffer from high amount of power consumption. Accordingly, the most investigations are focused on LC VCO design. Owing to the limited range of the varactors capacitance, the tuning range of LC VCOs is very narrow, especially in low frequency bands. However, many studies explore the tuning range of LC VCO but may do not meet the multi-band requirement such as tuning range, phase noise and power consumption.

Hsia has developed a multiband wide tuning range QVCO using p-mos only LC coupled VCO without any current source [6] resulting in high variation for current and power in different process corners. In this work, to achieve wide tuning range, switchable varactors and extra capacitors in different frequency band are used. Coupled and coupling transistor sizes based on small signal model including transistor noise sources for minimum phase noise amount have been optimized. This paper is organized as follows: section II gives the QVCO architecture and explains how it generates the required tuning range on desired frequency bands. Section III extracts the small signal model for complementary architecture and discusses the effect of each noise source on output phase noise. Section IV shows the time and frequency domains simulation results in ADS environment. Finally, section V offers the conclusions.

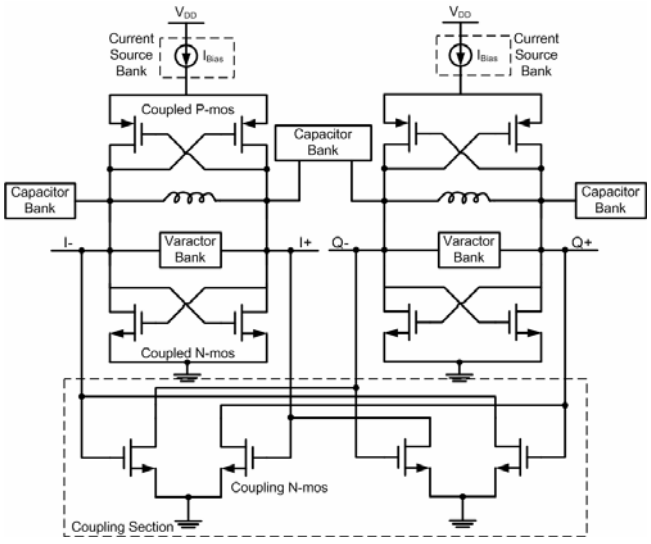

Figure 1. Complementary LC QVCO architecture.

II. QUADRATURE LC VCO ARCHITECTURE

A. VCO Core & Coupling Section

In order to generate the quadrature signal, coupled LC oscillator with switchable p-mos current source has been used, as it is shown in Figure 1. Considering this figure, VCO core consists of two independent complementary

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VCOs coupled to each other. Coupled p-mos and n-mos transistors make the structure symmetric, degrading the flicker noise impact on VCO phase noise. Meanwhile, negative resistance seen by output node is compensating more of the energy loss in LC tank and makes oscillation condition more facile. Considering required frequency bands, VCO gain has been chosen by 300MHz/V and has been kept constant, thus resulting in definite amount of thermal and flicker noise produced by Divider, PFD and Charge Pump block on total phase noise amount.

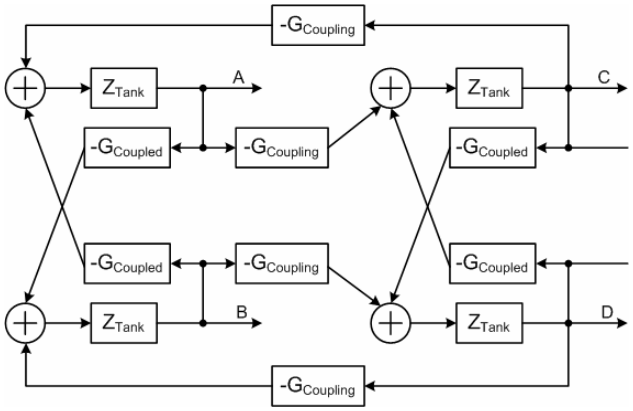

Figure 2. Linear quadrature model.

Assuming that the transistors in two cores are identical, there results in the trans-conductance of coupled and coupling devices as $g_{Coupled}$ and $g_{Coupling}$ respectively. The quadrature control loop can be modeled as shown in Figure 2 and the outputs will be [7]:

$$\begin{cases} A = \left(-g_{Coupled}.B - g_{Coupling}.C\right)\times Z_{Tank} \\ B = \left(-g_{Coupled}.A - g_{Coupling}.D\right)\times Z_{Tank} \\ C = \left(-g_{Coupled}.D - g_{Coupling}.B\right)\times Z_{Tank} \\ D = \left(-g_{Coupled}.C - g_{Coupling}.A\right)\times Z_{Tank} \end{cases} \quad (1)$$

Substituting $G = g_{Coupled}\times Z_{Tank}$ and $m = g_{Coupling}/g_{Coupled}$, equation (1) will be converted to the following matrix. The determinant matrix should be zero as to have non-zero answer.

$$\begin{bmatrix} 1 & G & m.G & 0 \\ G & 1 & 0 & m.G \\ 0 & m.G & 1 & G \\ m.G & 0 & G & 1 \end{bmatrix} \times \begin{bmatrix} A \\ B \\ C \\ D \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (2)$$

Equaling the determinant amount by zero $1\text{-}2G^2 + 4m^2G^2 + (1-m^4)G^4 = 0$, we have:

$$G = \frac{1}{1 \pm j.m} \Rightarrow \begin{cases} A = A \\ B = -A \\ C = \pm jA \\ D = \mp jA \end{cases} \quad (3)$$

Hence, on the condition which the matrix defined in (2) has a non-zero answer, the generated signals should have 90 degree phase difference. On the other hand, parameter *m* should be less than one, resulting in quadrature signals.

B. Control Scheme of Capacitor & Varactor Banks

One of the main challenges of multi-band/multi-phase VCO design is to extend/hop the narrow tuning range without degrading noise performance and keeping VCO gain constant. The proposed scheme is developed on the basis of a binary-weighted band-switching configuration by switching the extra capacitors in a capacitor bank. Besides that, each varactor tune-ability viewed as the ratio of maximum capacitance over the minimum amount limits by 2.5. Therefore, for keeping VCO gain constant, the varactor bank consisting of switchable parallel ones has been used as depicted in Figure 3. Additional capacitors have been implemented using Metal-Insulator-Metal (MIM) capacitors.

C. Current Source Bank

By changing the frequency band toward higher frequencies, quality factor (Q) of inductor is increased resulting in more signal swing and easier oscillation state.

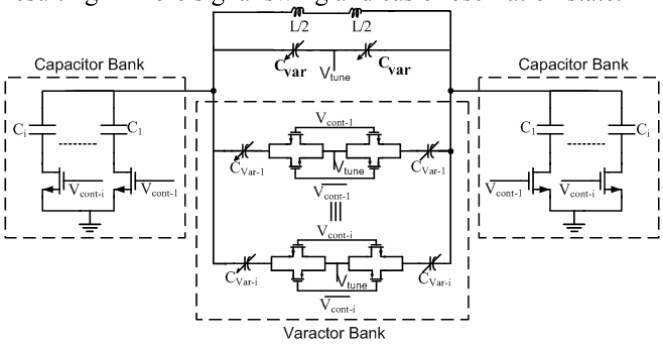

Figure 3. Varactor and capacitor banks.

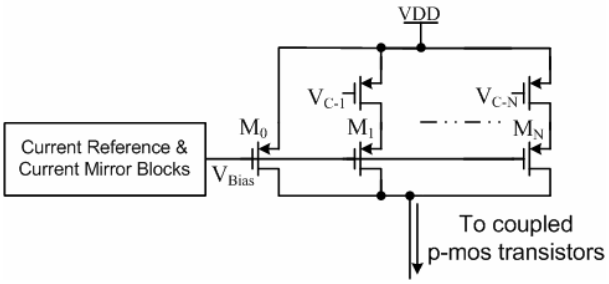

Figure 4. Current source bank.

In this situation, smaller amount of current is required to obtain desired signal swing and phase noise. On the other hand, by increasing signal swing, the oscillator could enter in a voltage limited region, and degrade the phase noise. Thus, it is preferable to control and optimize the total current that id injected into oscillator in different frequency bands. Figure 4 shows current source bank including fixed M0 and switchable transistors.

III. Small Signal Model and Paremeters Optimization

Using coupling section between two VCO cores and generating quadrature signals (according to (3)), total phase noise is exacerbated by two interfering factors:

A. Decreasing Coupled N-MOS Transistors Current

According to Figure 1, DC current coupling section consisting of n-mos transistors is drawn from coupled p-mos transistors, thus resulting in different currents for coupled n-mos and p-mos transistors and asymmetric structure. In this case, oscillations signal rising and falling edges are not

equal, resulting in more phase noise on output node.

B. Noise Injection from One Stage to Another

By coupling both VCO cores, the coupling section injects the uncorrelated thermal and flicker noise of each stage into another. Consequently, noise power of each stage will be integrated, resulting in more phase noise on output node. Harmonic balanced phase noise simulation is useful for predicting the accurate phase noise but this will be too complex to help a chip-designer to understand the VCO operations. However, a linear phase noise model is simple and gives useful insight into the phase noises. Figure 5 represents the linear model of complementary QVCO architecture in which $I_{np\text{-}Current}$, I_{nn}, I_{np} and I_{nc} represent noise source of current source block, coupled and coupling transistors respectively. The LC thank is modeled with R_T, C_T and L_T and Ks is the coupling factor between two VCO cores (0<Ks<1) which is zero in a conventional VCO [8]. By increasing this parameter, open loop gain and total trans-conductance seen by each output node will be increased. As long as, all noise sources are uncorrelated, the output power of LC tank is described as the superposition of all the noise sources power resulting in power spectral density of:

$$\overline{V_O^2} = \left(\alpha_{nn}^2 . \overline{i_{nn}^2} + \alpha_{np}^2 . \overline{i_{np}^2} + \alpha_{nc}^2 . \overline{i_{nc}^2} + \alpha_{p\text{-Current}}^2 . \overline{i_{p\text{-current}}^2} + \alpha_T^2 . \overline{i_{nT}^2} \right) \quad (4)$$

where α is noise contribution coefficient or impedance seen by each noise source. In order to see the effect of each noise source on output noise power, each noise source coefficient should be calculated separately, which would be:

$$\alpha_X = \frac{P}{1 + C_{Total}.s.P/2 - g_{mT}.P/2}, \quad \begin{cases} g_{mT} = g_{mn} + g_{mp} + K_S.g_{mc} \\ C_{Total} = \sum_{i=1-3} C_{db\text{-}i} + \sum_{i=1-3} C_{gs\text{-}i} \end{cases} \quad (5)$$

where P is the total impedance of tank ($P = R_T || 1/C_T.s || L_T.s$), g_{mT} and C_{Total} are the total trans-conductance and total capacitance amount seen by output nodes respectively. According to equations (4) and (5), the more trans-conductance or tank impedance (P), the more output noise power and the more signal amplitude resulting in more SNR and less phase noise amount. Hence, the more inductor quality factors, the less total phase noise will be. Notice that by increasing one of the two mentioned factors resulting in more amplitude, oscillator should not enter voltage limited regime corrupting phase noise. According to (5), g_{mT} consists of trans-conductance of each coupled transistor and coupling section. By increasing the trans-conductance of coupling transistors, signal amplitude will not increase, resulting in more phase noise. Thus, coupling section current should be chosen as low as possible polling just the two VCOs in 90 degree phase difference. On contrary, the sizes of these transistors should not be selected too low, as far as flicker noise power is inversely proportional with transistor sizes. In order to optimize the power consumption for phase noise amount, the oscillator should be designed as symmetric as possible. Equation (6) shows the phase noise generated by thermal noise on specific frequency offset of Δw [9]:

$$L(\Delta w) = 10.\log\left(\frac{\Gamma_{rms}^2}{q_{max}^2} . \frac{\overline{i_n^2}/\Delta f}{4.\Delta w^2} \right), \quad \Gamma(x) = V_i'(x)/V_{i\text{-}max}'^2 \quad (6)$$

where q_{max} is the maximum charge on tank capacitor, Γ_{rms} is root mean square of effective impulse sensitivity function of oscillator structure and $\overline{i_n^2}/\Delta f$ is noise PSD amount.

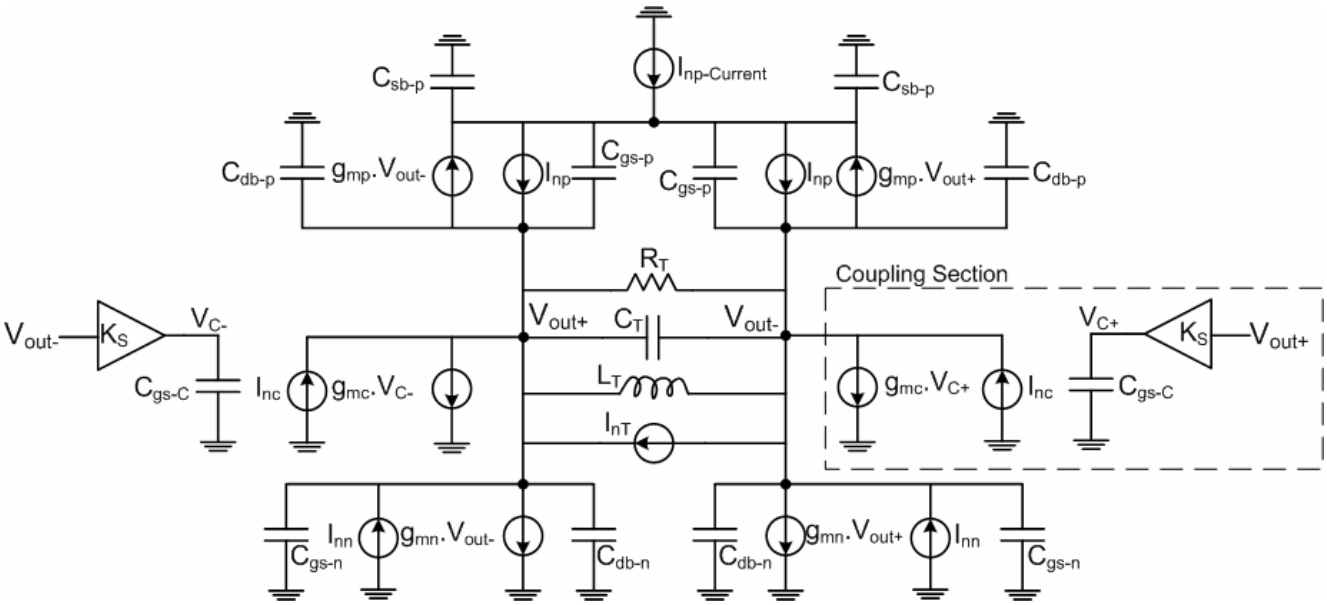

Figure 5. Equivalent circuit of complementary QVCO with noise sources.

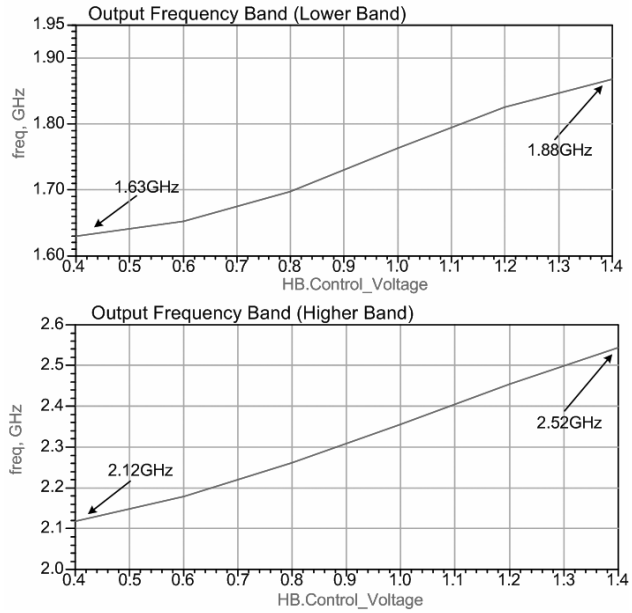

Figure 6. Output frequency spectrum versus tuning voltage.

Replacing Γ_{rms} by its Fourier series, phase noise resulted by flicker noise will be:

$$L(\Delta w) = 10.\log\left(\frac{c_0^2}{q_{max}^2}.\frac{\overline{i_n^2}/\Delta f}{8.\Delta w^2}.\frac{w_{1/f}}{\Delta w}\right), \qquad (7)$$

$$c_0 = \frac{1}{\pi}\int_0^{2\pi}\Gamma(x).\alpha(x)$$

where $w_{1/f}$ is corner frequency of device flicker noise. According to (7), the less C_0, the less phase noise will be. By choosing the output common voltage as $V_{DD}/2$ in the complementary structure, $\Gamma(x)$ will be symmetric. α(x) is the portion of each noise source in one period of output waveform. As long as in each half cycle of output signal, one of the coupled n-mos transistors and one of the coupled p-mos transistors are ON, α(x) will be symmetric but for the most noise degradation n-mos and p-mos coupled transistors trans-conductances should be equal. For a given power dissipation for the oscillator, coupled p-mos transistor sizes should be selected resulting in appropriate signal swing. In this case, on output signal peak, the oscillator should remain in current limited regime. Total definite p-mos current amount will be flown through coupled and coupling transistors. Having selected coupling transistors based on previous explanations, coupled n-mos transistor current will be:

$$I_{N\text{-Coupled}} = \frac{(W/L)_{Coupled}\times I_P}{(W/L)_{Coupled}+(W/L)_{Coupling}} \qquad (8)$$

Based on (8) and equating gate-source voltages, we have:

$$K_N.(W/L)^2_{Coupled} - A_P.(W/L)_{Coupled} - A_P.(W/L)_{Coupling} = 0 \quad (9)$$

where $A_P = K_P.(W/L)_P$. In this situation, coupled n-mos transistor sizes extracted by (9) result in the least amount of flicker noise on output phase noise.

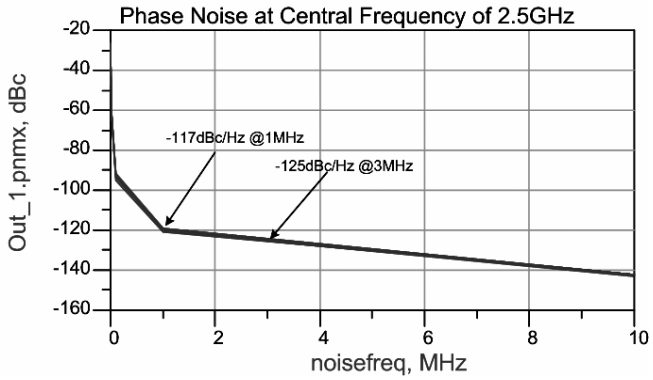

Figure 7. Phase noise at different frequency offsets.

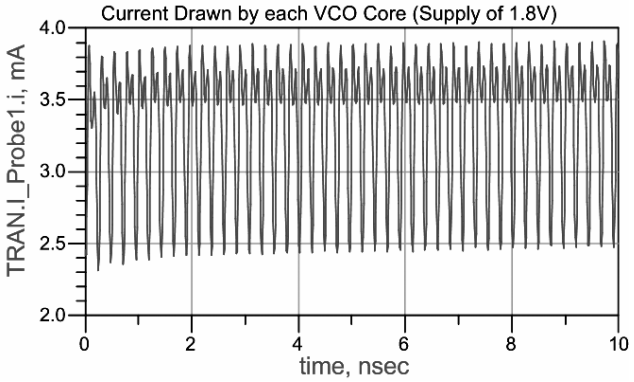

Figure 8. Current drawn by each VCO core.

IV. Simulation Results

The proposed QVCO was implemented by TSMC RF 0.l8um CMOS technology in ADS environment with a supply voltage of 1.8V. QVCO control voltage tuning range has been selected between 0.4V – 1.4V. By switching the external capacitor bank, two frequency bands of 1.65-1.85GHz and 2.4-2.5GHz were achieved, as illustrated in Figure 6. In order to cover the total frequency range of 1.6-2.5GHz, external switchable capacitors have been used. According to this figure, the smallest frequency is 1.63GHz, obtained when all of external capacitors are applied and the highest frequency is 2.52GHz when the output external capacitor is 225fF. On the other hand, it can be seen that the VCO gain at lower and higher band is 250MHz/V and 400MHz/V respectively. At 1MHz and 3MHz frequency offsets, the phase noise of proposed QVCO at central frequency of 2.5GHz has been measured as -117dBc/Hz and -125dBc/Hz respectively as shown in Figure 7. The current switches are controlled in order to keep the power consumption constant for two desired frequency bands. Figure 8 shows the current drawn by each VCO core from the supply voltage of 1.8V. According to this figure, the mean of current drawn by each VCO is 3.25mA. The extracted total current consumption, including two VCO cores and buffer blocks, is 7.5mA resulting in 13.5mW power. Usually Figure of Merit (FOM) in a VCO is defined by [10]:

$$FOM(dB) = L(Offset) + 10.\text{Log}\left(\frac{P_{DC}}{1mW}\right) - 20.\text{Log}\left(\frac{f_{Osc}}{f_{Offset}}\right) \qquad (10)$$

TABLE I. PROPOSED AND PREVIOUS WORKS PERFORMANCE COMPARISON

Design	Supply Voltage (V)	Process	Frequency Range (GHz)	Phase Noise	Power (mW)
M. Hsia [7]	1V	0.18um CMOS	0.89 – 2.5	-139dBc/Hz @ 3MHz	31
L. Perraud [11]	1.3V	0.18um CMOS	8.5 – 10.73	-96dBc/Hz @ 100kHz	14
This Work	1.8V	0.18um CMOS	1.63 – 2.52	-125dBc/Hz @ 3MHz	13.5

Achieved FOM for implemented QVCO at frequency offset of 3MHz is -176dB at 2.4GHz. Table I lists the comparison results of the proposed and conventional multi-band VCOs. From this table, proposed QVCO demonstrates a fairly good performance to realize multi-band applications at low power consumption.

V. CONCLUSION

In this work, we proposed a low power dual band LC QVCO operating at a supply voltage of 1.8V for RFID, Zigbee and Bluetooth applications using 0.18um CMOS technology. The proposed QVCO architecture using external capacitor bank, varactor bank, current source bank is designed to yield quadrature output signal at multiple frequency bands by keeping the total drawn current as low as possible. A small signal model including noise source of each transistor and their effect on output noise was presented. On the basis of described analysis, the optimum amount of coupling n-mos and coupled transistors' sizes were extracted. According to simulation results, phase noise of the proposed QVCO with the achieved amount of -125dBc/Hz at offset of 3MHz can satisfy the requirements of desired communication standards while its power consumption remains at 13.5mW.

REFERENCES

[1] "IEEE Standard 802.15.1-2002", IEEE Standard for Information technology - Specific requirements Part 15.1: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Wireless Personal Area Networks (WPANs).

[2] "Specification of Bluetooth systems", Bluetooth standard publications, February 2001.

[3] U. Karthaus, "Fully integrated passive UHF RFID transponder IC", IEEE J. Solid-State Circuits, vol. 38, pp. 1602-1608, October 2003.

[4] R. Sheen, and C. Chen, "A wide-range phase-locked loop using a range-programmable voltage-controlled oscillator", Proc. of IEEE 43th Midwest Symp. Circuits and Systems, vol. 1, pp.526-529, August 2000.

[5] C. Chen, and R Sheen, "A power-efficient wide-range phase-locked loop", IEEE J. Solid-State Circuits, vol. 37, pp. 51-62, January 2002.

[6] M. Hsia, and O. Chen, "A multiband CMOS LC Quadrature VCO for GSM/DCS/DECT and Bluetooth Systems", IEEE International Symposium of Circuit and Systems, May 2006.

[7] J. Wang, J. Tan and O. Wing, "A Theory of cross coupled oscillator system for RF Quadrature generation", Proc. of IEEE International Conference of Circuit and System for Communication, pp-362-265, 2002.

[8] S. Ko, and S. Hong, "Noise property of a Quadrature balanced VCO", IEEE Microwave and Wireless Components Letters, vol. 15, no. 10, October 2005.

[9] A. Hajimiri, and T. H. Lee, "A general theory of phase noise in electrical oscillators", IEEE J. Solid-State Circuits, vol. 33, no. 2, February 1998.

[10] L. Perraud, L. Bonnot, N. Sornin and C. Pinatel, "Fully integrated 10 GHz CMOS VCO for multi-band WLAN applications", Proc. of Europe Solid-State Circuits Conf, pp. 353-356, September 2003.