Power Factor Improvement in Switched Reluctance Motor Drive

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***Abstract*—A Switched Reluctance Motor (SRM) drive is a variable speed motor drive system with unique characteristics. The switching of voltage into the phase winding and pulsating AC input current leads to low power factor and high harmonic contents. In this paper, the power factor is improved using boost converter. The hardware results are taken for a DC input voltage of 60 V to the SRM with different load currents. From the results, it is found that the total current harmonic distortion and individual current harmonics are less with Power Factor Controller (PFC). The power factor of the circuit is improved with the proposed power factor controller.**

***Index Terms*—Switched Reluctance motor, Boost converter, Power factor control, Harmonics**

I. INTRODUCTION

The structure of SRM is simple, with salient poles on both stator and rotor. It has no windings or magnets on the rotor. The operation of the SRM is based on the principle that the rotor will always try to align its poles with the position which provides minimum reluctance for the magnetic circuit. SRM is suitable for variable speed as well as servo type applications. The operation of SRM and its controllers are explained in detail by Lawrenson P J [1], Miller [2] and Krishnan R [3].

Barnes et al improved the power factor of 4/2 pole SRM by reducing the capacitor voltage ripple and peak phase current [4]. Corda and Oljada discussed about various converter circuits and switching circuits of SRM [5]. Krishnan and Lee described the power factor correction circuit by sensing the DC link voltage to control the boost converter switch [6]. Lee S discussed the impact of PFC circuit in switched reluctance motor, permanent magnet brushless DC motor and DC motor [7]. Xue X D et al discussed about the effects of control parameters and outputs of SRM drive systems on power factor through simulation and experimental analysis [8, 9]. Jurgen Reinert et al discussed the power factor correction for SRM drives with diode bridge rectifier with stable DC link voltage, pulsating DC link voltage and step up converter [10]. Beno et al improved the power factor by optimizing the switching angles of SRM [11]. Kumar et al explained the fuzzy tuned PID controller based PFC for SRM drive [12].

The literature survey reveals that there is a possibility to improve the power factor of the switched reluctance motor with asymmetric bridge converter. The asymmetric bridge converter is used to switch the current in the phase windings. The switching of voltage into the phase winding is done by power converter, in which the input current is distorted. It draws a pulsating AC line current, resulting in low input power factor and high harmonic line current. The distortion of the current leads to the reduction of the quality of power supply.

In this paper, a boost converter method is introduced to improve the power factor. The voltage follower stage consists of inverter; transformer and rectifier are used to reduce the boost converter output voltage to machine operating voltage at lower levels. The hardware results are taken for an input DC voltage of 60 V to SRM and for various load currents.

II. POWER FACTOR CONTROLLER CIRCUIT

The conventional SRM drive consists of rectifier, filter and machine converter circuit. In the proposed power factor controller, a boost and voltage follower is introduced to minimize the distortion of the line current switched into the windings of SRM, as shown in Figure 1. The boost converter, as shown in Figure 2, is used as power factor controller. It is designed to operate from the single phase supply for an output voltage of 400 V DC.

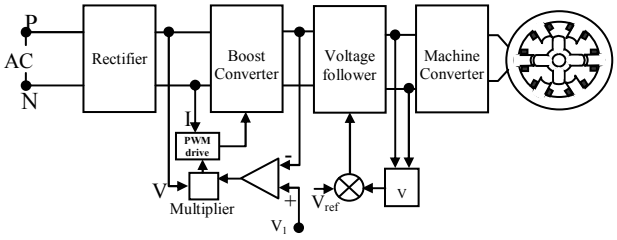

Figure 1. Schematic diagram of SRM with power factor controller.

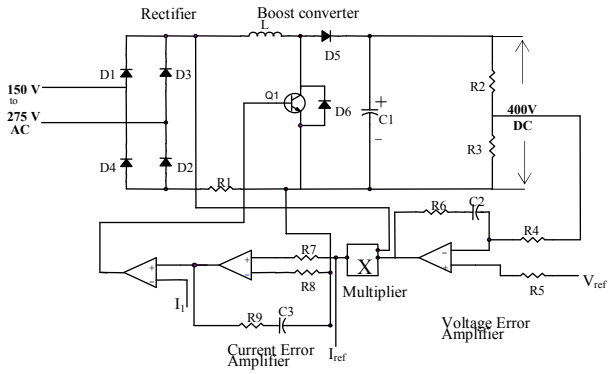

Figure 2. Boost converter.

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A. Input Inductor design

The inductor is designed to limit the peak ripple current or change in current (ΔI) within 20 % of the peak input current. The selection of inductor value is based on Duty cycle (D), input voltage (V_{in}), switching frequency (f_s) and change in current (ΔI). The inductance is given by,

$$L = \frac{V_{in}\sqrt{2}.D}{f_s.\Delta I} \quad (1)$$

The value of Duty cycle is calculated from minimum input voltage ($V_{in(min)}$) and output DC voltage of the boost converter (V_0) and it is given in Equation 3.

$$D = \frac{V_0 - V_{in(\min)}}{V_0} \quad (2)$$

The calculated value of Duty cycle for the boost converter is 0.469. Here, the value of the $V_{in(min)}$ and V_0 are considered as 150 V and 400 V respectively.

The change in current is calculated from 20% of the line current (peak value). The line current ($I_{line\ (peak)}$) is designed from the output power (P_{out}), rms value of minimum input voltage ($V_{in\ (min)}$) and efficiency (η) of the converter circuit and their relationships are given in equation 3. In practice, the maximum percentage efficiency of the converter circuits is considered as 90 % and the same is considered for the analysis. The power output of the SRM drive is 1.2 kW.

$$I_{line\ (peak)} = \frac{\sqrt{2}\,P_{out}}{V_{in\ (\min)}\,\eta} \quad (3)$$

The calculated value of the $I_{line\ (peak)}$ is 12.57 A.

The switching frequency of the boost converter is considered as 50 kHz. The designed value of inductor in the boost converter is 0.791 mH.

B. Output capacitor design

The output capacitor (C_o) is selected depending on factors such as switching frequency (f_s), ripple current, DC output voltage(V_o), Minimum output voltage ($V_{o(min)}$) and the holdup time(Δt). The total current through the output capacitor is the RMS value of the switching frequency ripple current and the second harmonic of the line current.

$$C_o = \frac{2P_{out}\Delta t}{V_o^2 - V_{o(\min)}^2} \quad (5)$$

The calculated value of the output capacitor is 640 μF.

C. Design of Zero voltage switching (ZVS) DC-DC converter

This section describes the conversion of the PFC output of 400 V DC to required maximum output of 160 V, as shown in Figure 3. It also provides isolation between input side and output side. It operates in variable frequency resonant mode zero voltage switching. In the half bridge, the peak voltages are clamped to the DC input link voltage. It will reduce the switch voltage stress as compared to single ended converters operating in resonant mode zero voltage switching conditions.

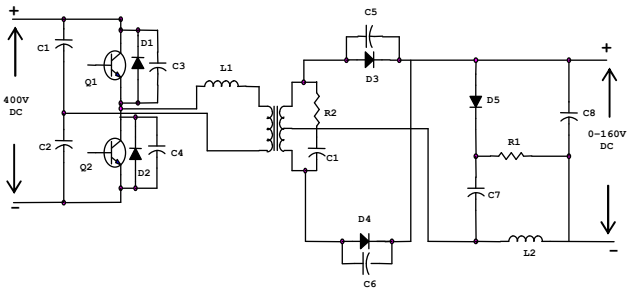

Figure 3. ZVS DC-DC converter.

The resonant frequency (f_r) of the converter circuit is given by,

$$f_r = \frac{1}{2\pi\sqrt{L_r 2C_r}} \quad (6)$$

The values of resonant inductance (L_r) and resonant capacitance (C_r) are chosen as 40 μH and 4.7 nF. The resonant frequency of the circuit is calculated as 367 kHz.

III. Experimental Results

The SRM is coupled with a DC shunt generator and the hardware results are taken for DC input voltage of 60 V with different load currents. The applied input voltage, input current, input power factor and input Total current Harmonic Distortion (THD) are measured for different load currents. Table I shows power factor and percentage total current harmonic distortion for various load currents. Figure 4 shows the comparison of various load current and power factor with and without power factor controller. The power factor of the circuit without PFC ranges from 0.57 to 0.67 for a load current range of 1.2 A to 5.02 A. The power factor of the circuit improves from 0.86 to 0.96 for a load current range of 1.2 A to 5.02 A.

The various load currents and its percentage THD values are measured and it is found that the percentage THD value is reduced to 13.6 from 103.8 for the load current of 4.8 A, as shown in Figure 5. Figure 6 shows the comparison of Individual harmonic limits up to 13th harmonics. The individual harmonics is also reduced with the power factor controller.

From this analysis, it is observed that the power factor of the circuit is improved and current THD value of the system is reduced with the proposed power factor controller. The individual harmonics of the system is also reduced with the power factor controller.

TABLE I. POWER FACTOR AND % THD FOR VARIOUS LOAD CURRENTS AT DC INPUT VOLTAGE OF 60 V

Load current	Power factor		% THD	
	Without PFC	With PFC	Without PFC	With PFC
1.2 A	0.57	0.86	107.2	16.5
2.86 A	0.61	0.90	114.3	11
3.81 A	0.62	0.92	112.6	14.5
4.8 A	0.63	0.94	102.8	13.6
5.02 A	0.67	0.96	107.8	11.1

Figure 4. Comparison of load current vs. power factor.

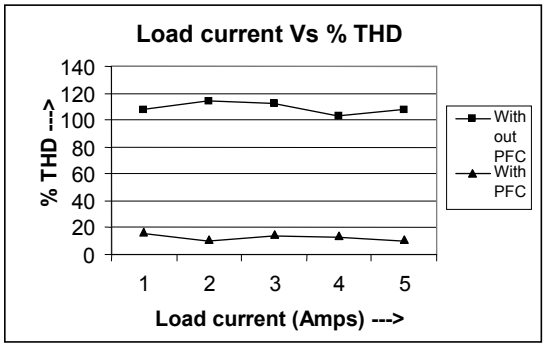

Figure 5. Comparison of load current vs. % THD.

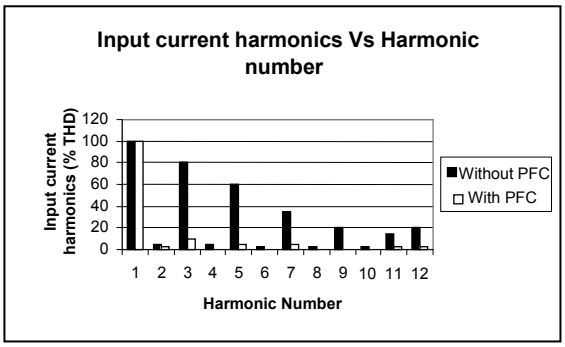

Figure 6. Comparison of Input current harmonics and Harmonic number.

The Figures 7 and 8 show the hardware results with and without power factor controller. It consists of the voltage and current waveform, current harmonic spectrum and power details for a SRM input DC voltage of 60 V and for a load current of 4.8 A.

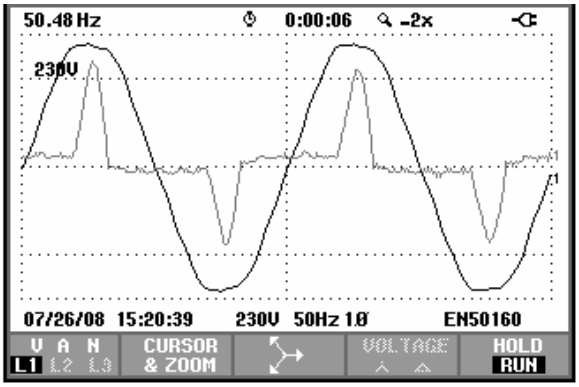

Figure 7. (a) Current and voltage waveform.

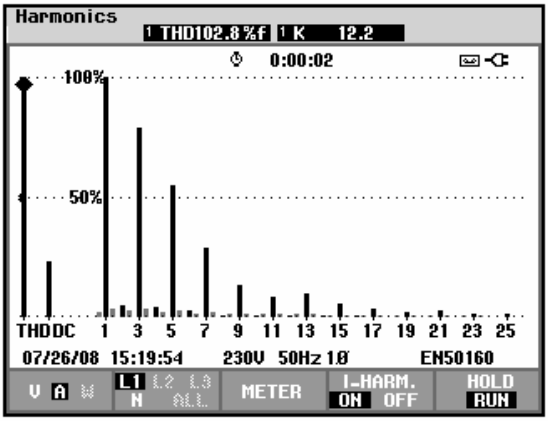

Figure 7. (b) Current harmonics spectrum.

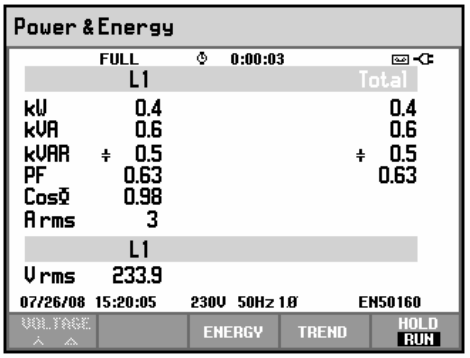

Figure 7. (c) Power details.

Figure 7. Experimental results without power factor controller.

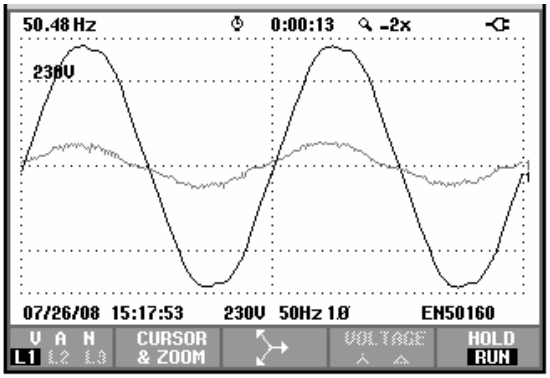

Figure 8. (a) Current and voltage waveform.

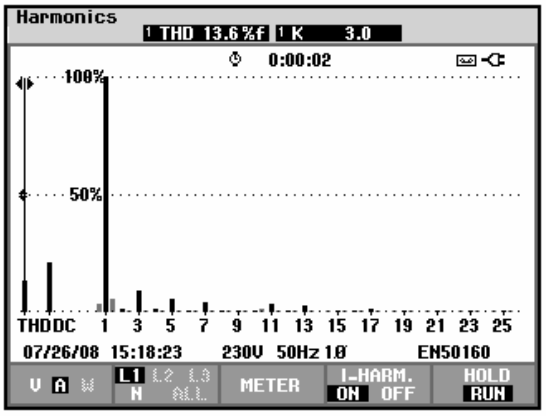

Figure 8. (b) Current harmonics spectrum.

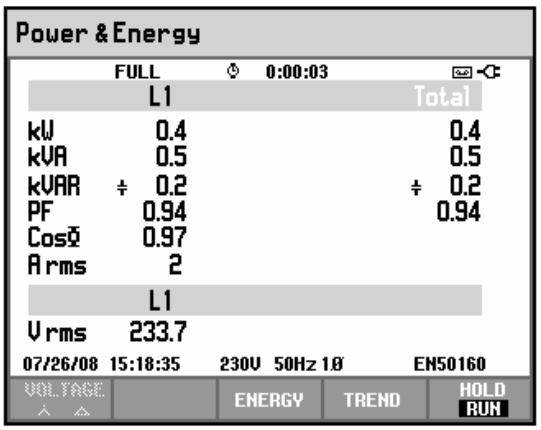

Figure 8. (c) Power details.

Figure 8. Experimental results with power factor controller.

From Figures 7 and 8, the input current waveform is improved with the proposed power factor controller and it is nearer to sinusoidal. The percentage current THD and individual harmonics are also reduced. The power factor of the circuit improves with the proposed power factor controller.

IV. CONCLUSION

In this paper, a SRM drive system with power factor controller circuit is designed and implemented. The hardware results are taken for a DC input voltage of 60 V to the SRM and various load currents. From the results, the total current harmonic distortion and individual current harmonics are very litlle with power factor controller. The power factor of the circuit is improved with the proposed power factor controller. The improvement in the power factor increases the overall efficiency of the system.

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