Basic Consideration for Signal Processing Solutions Used in Sigma-delta Based ADC and DAC Converters

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***Abstract*—During the last decade there was an explosion in the field of mobile multimedia devices that led to the emergence of new and very complex requirements for the producers of integrated circuits (IC's). Practically, many of the difficulties localized in the systems made with multiple discrete IC's have moved one level down, inside the IC itself (this is how the concept of System on Chip came up). This paper presents exactly such an example in which the audio section of a mobile phone must coexist with the intermediate radio frequency section in a single IC. It starts by mentioning the technical challenges facing this request, followed by an introduction of the fundamental theories used in finding the most efficient solution.**

***Index Terms*—CIC, mobile phone audio subsystem, multirate filtering, sample rate converter**

I. Introduction

This paper will start with some background information about the mobile phones architectures, which will allow the reader to understand how the need of performing fractional decimation and interpolation has arisen. This can also be called Sample Rate Conversion (SRC) because the input signal coming at a certain sampling frequency is changed into the same signal but with different sampling frequency.

The decimators and the interpolators are classic blocks inside any Analog to Digital Converter (ADC) or Digital to Analog Converter (DAC) based on sigma-delta modulation principles. Up until a few years ago, the ratio of interpolation and decimation were always integer numbers. This means that the actual frequency for an audio chip working at 44.1 kHz (the CD standard) for example, needed to be a multiple of that frequency. A chip designed for a telephony voice application that uses 8 kHz will need a different clock frequency. The only way to create a chip having a single clock frequency that covers these two standards is either to incorporate internally a PLL or to try a digital solution, like the one that will be shown in this paper.

II. Typical Architecture Of A Mobile Phone

The most important blocks inside a mobile phone are presented in

Figure 1. We see the analog blocks that make the interface with the signal from the surrounding world (audio signals, video signals and radio frequency signals) and the digital blocks that perform most of the signal processing required. All these need to communicate somehow. Since there is a long history and legacy for each of the applications that are now all incorporated in a single phone, it's quite normal to have several challenges when trying to interconnect them. The aspect that will be of relevance in our case and which will be further analyzed in this document, regards the requirement of having a MCLK (Master clock) of 13 MHz inside the mobile phone for the RF section and that should also be used for the rest of the sections.

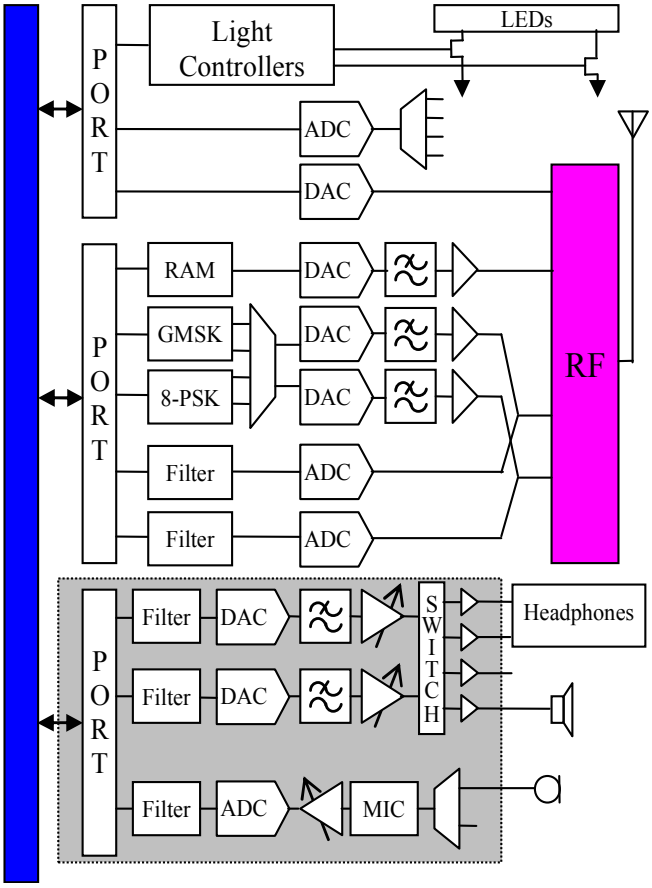

Figure 1. **Top level architecture of a basic mobile phone.**

Digital Object Identifier 10.4316/AECE.2010.01013

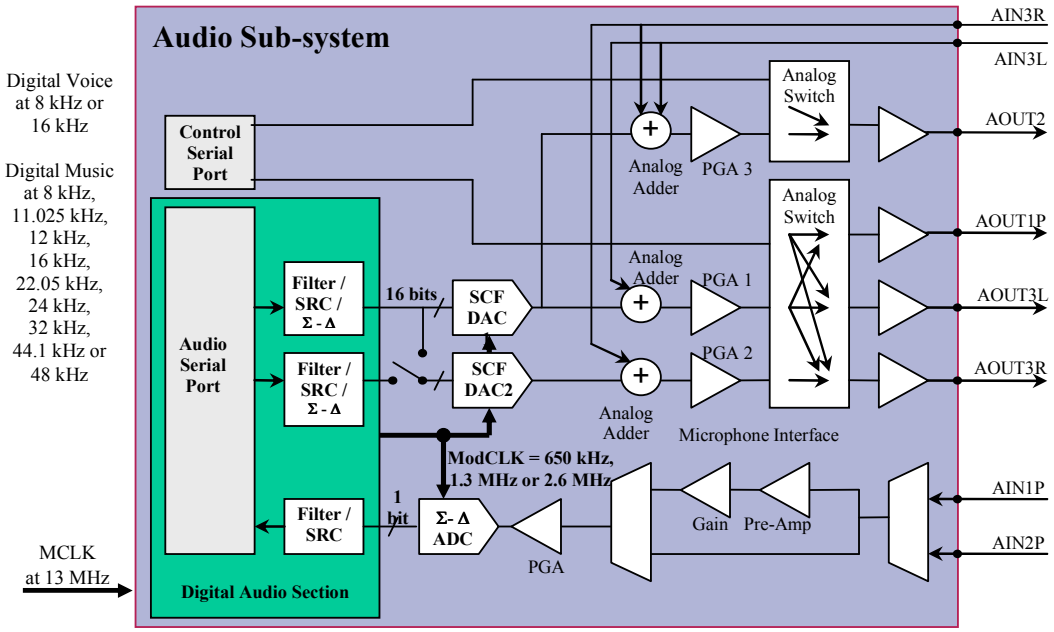

Figure 2. Architecture of an audio sub-system inside a mobile phone.

The digital section of such converters, based on sigma-delta modulation techniques, becomes much more important and complex than in other types of converters. There is also a lot of signal processing performed in the process of interpolation for the DAC channels or decimation for the ADC channel. The two sample rate converters are shown in yellow (Figure 3).

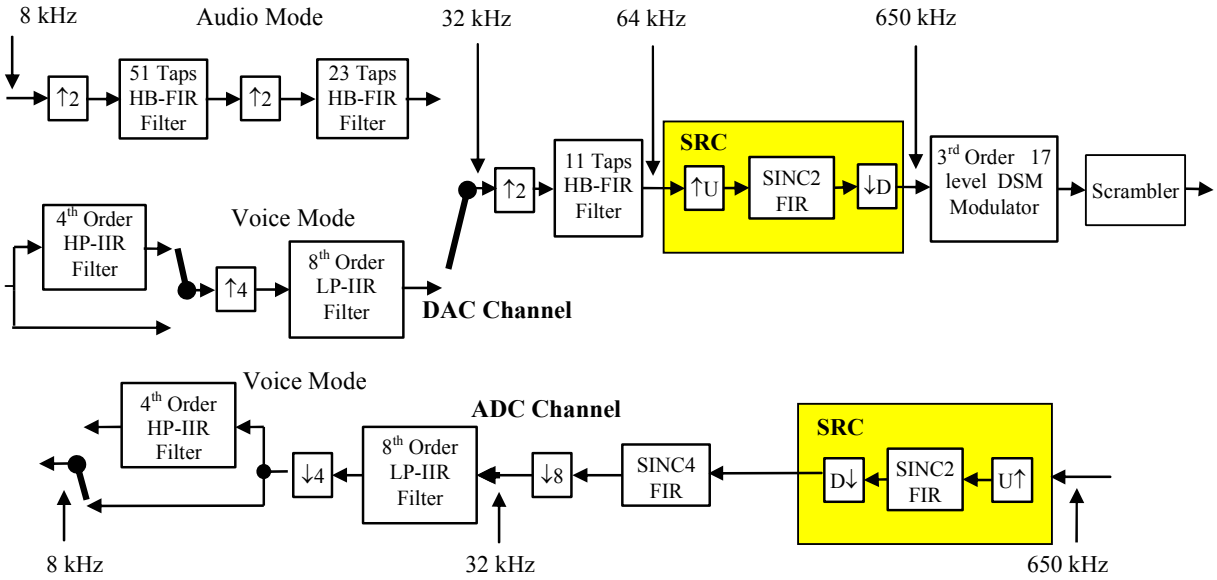

Figure 3. Digital section of the audio sub-system.

III. THE SAMPLE RATE CONVERTERS

Like it was mentioned earlier, the value of the master clock for the audio digital section is 13 MHz and this value is dictated by the Intermediate Radio Frequency section of the chip that needs to comply with the GSM standard requirements. This value is not a good one for the audio subsystem because it's not an integer multiple of any of the existing standard audio sampling rates.

Obviously, the phone manufacturer can use a dedicated crystal just for the audio subsystem, but that will make the microchip more complex, it will require an extra crystal and it will lead to several clock domains inside the same microchip causing other problems. Another solution can be the use of a dedicated PLL, but this is a pretty expensive one and can become quite complex since it needs to cover so many standard audio sampling rates.

This is why a lot of effort has been made to find good digital architectures that will solve this problem entirely in the digital domain using any value of frequency within a certain range.

Basically, the block that can do this is called a sample rate converter and it has this general description of the function performed: if a signal is received at the input with the sampling frequency Fs_in, it should be converted to the

same signal, but sampled at the frequency Fs_out, while a certain amount of information, usually in a limited band, must be preserved.

Since the signals that we are dealing with are in the digital domain, it makes sense that the techniques to perform the SRC are implemented in the digital domain, as well.

Yet, this process can be understood easier using the idea of re-sampling after reconstruction:

An analog signal is (virtually) reconstructed from the digital signal by means of D-to-A conversion and filtering.

Eventually the reconstructed signal is re-sampled with the desired frequency and a new digital signal is obtained by means of A-to-D conversion.

From this idea, the all-digital description of the process can be obtained, keeping in mind that SRC is a process of re-sampling. The fundamental effects of sampling, imaging and aliasing, must be expected to appear with SRC.

A. Signal Flow in a SRC

The most straightforward solution for an SRC module is to reconstruct the original analog signal from the discrete-time signal and resample the reconstructed signal with the new clock period [1].

The fundamental effects of sampling, imaging and aliasing, must be expected to appear with SRC, making it to be mainly a problem of designing appropriate (anti-imaging and anti-aliasing) filters and hardware structures to implement these filters.

The big advantage of this method depicted in the image below (Figure 4), is that it works for absolute any ratio of input sampling frequency (Fs_in) to output sampling frequency (Fs_out).

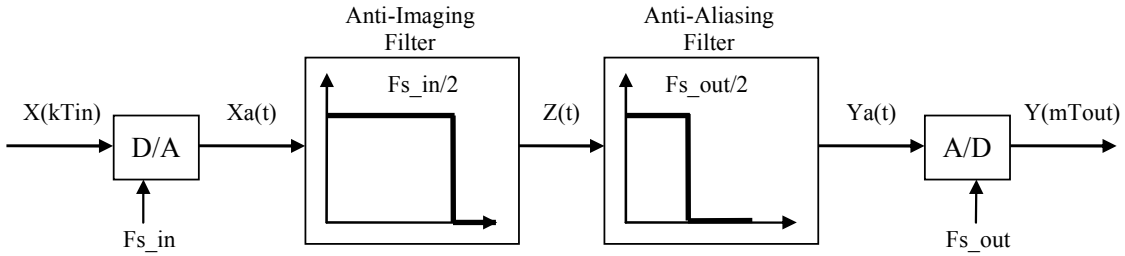

Figure 4. Conceptual diagram of an ideal Sample Rate Converter.

where:
X(kTin) = original signal in the discrete-time domain sampled with the frequency Fs_in;
Xa(t) = original signal in the continuous-time domain;
Z(t) = reconstructed signal from the original one in the continuous-time domain;
Y(t) = anti-aliased signal for new sampling in the continuous-time domain;
Y(mTout) = re-sampled signal in the discrete-time domain with the frequency *Fs_out*;

Several limitations are associated with this method:

1. In order to keep the large signal-to-noise-ratio (SNR), very high quality D/A and A/D converters have to be used.
2. The output signal of the D/A converter must be reconstructed by a high precision analog anti-imaging filter with cutoff frequency Fs_in/2, in order to remove all the images due to D/A conversion.
3. To fulfill the Nyquist theorem requirements, the input signal of the A/D converter must be band-limited to *Fs_out*/2 by an analog anti-aliasing filter.
4. Any jitter on the sampling clocks will translate into signal distortion and thus, it needs to be suppressed by additional circuitry.

If the output sample rate Fs_out is larger than the input sample rate Fs_in (sampling rate is increased), the second filter can be omitted. In the opposite case (sampling rate is decreased) the first filter is not necessary. Therefore both low-pass filters can be merged into one (Figure 5) with the cutoff frequency given by the following expression:

$$Fcutoff = \begin{cases} Fs\_in/2, \text{ if } Fs\_out > Fs\_in \\ Fs\_out/2, \text{ if } Fs\_out > Fs\_in \end{cases} \quad (1)$$

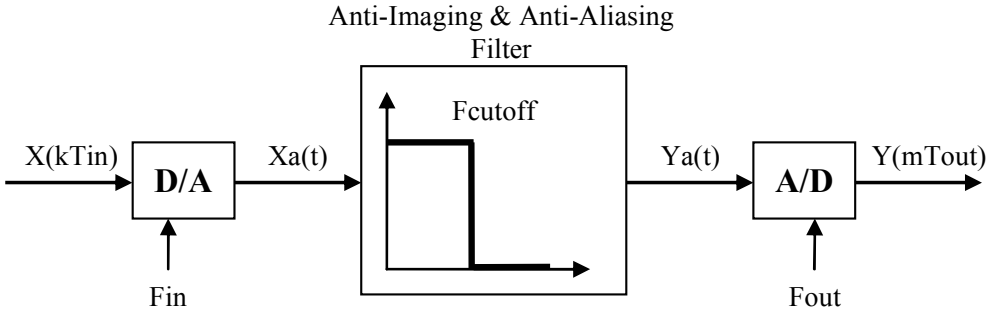

Figure 5. Optimized diagram of the ideal SRC.

This anti-imaging & anti-aliasing filter, which must be realized in the analog domain, needs a flat pass-band, a narrow transition band and a highly attenuated stop-band. The required specifications make the problem hardly solvable.

Many of the above problems can be avoided by

performing the sample-rate conversion process in the digital domain. The A/D and D/A converters can be omitted and the analog filters are replaced by digital ones.

B. Digital-Domain Solution

The description of the SRC using the analog-domain solution is appropriate to easily understand the process, but in terms of practical implementations, there are some major disadvantages. Moreover, since the input and the output of the module are discrete-time signals, a solution that will keep the full signal flow in the digital domain is more appropriate.

The problem of an accurate reconstruction of the input signal that was faced in the analog-domain solution is therefore changed into a problem of an accurate interpolation. A variety of algorithms for interpolation can be used at this stage, each one having its own advantages and disadvantages.

Interpolation is a well-known solution to the mathematical problem of calculating in-between values of tabulated functions. In the context of signal processing the table elements are replaced by signal samples. However, when comparing the requirements for calculating in-between values of tabulated functions and for calculating those of discrete-time signals, it becomes obvious that the typical approach of using interpolation for SRC is not sufficient.

The classic idea of interpolation is to have a smooth curve whose samples are tabulated values, making this process a time-domain approximation. In signal processing, the constraints on calculating in-between values can be different. The main concern is the information carried by the signal or parts of it. To understand this, it is helpful to shift the point of view from time to frequency domain. By doing this, the requirement for SRC can be formulated as calculating in-between values of discrete-time signal such that a certain frequency band of the signal is not distorted. The standard approach of this problem is performing the following two major steps:

1. A very good technique to be employed in the interpolation algorithms is to use the idea of up-sampling followed by an appropriate filter. The up-sampling value will depend on the desired conversion rate. Generally, this number is so big, that we can think of the new signal as being a pseudo-analog one.
2. The next step in the case of the analog-domain solution was to resample the signal at the desired rate. In the digital-domain this is replaced by down-sampling or decimation process. Of course, we are to ensure that the signal is band limited to half of the resulting sampling frequency. This will be the role of another low-pass digital filter.

In the end, we obtain the following block diagram of a SRC module (Figure 6) in the digital domain [2] (note that the interpolation must precede the decimation to keep the maximum bandwidth of the input signal).

The two low-pass filters can be merged into a single one with a cutoff frequency obtained in the same way as the analog implementation (Figure 7).

$$Fcutoff = \begin{cases} Fs\_in/2, \text{ if } Fs\_out > Fs\_in \\ Fs\_out/2, \text{ if } Fs\_out > Fs\_in \end{cases} \quad (2)$$

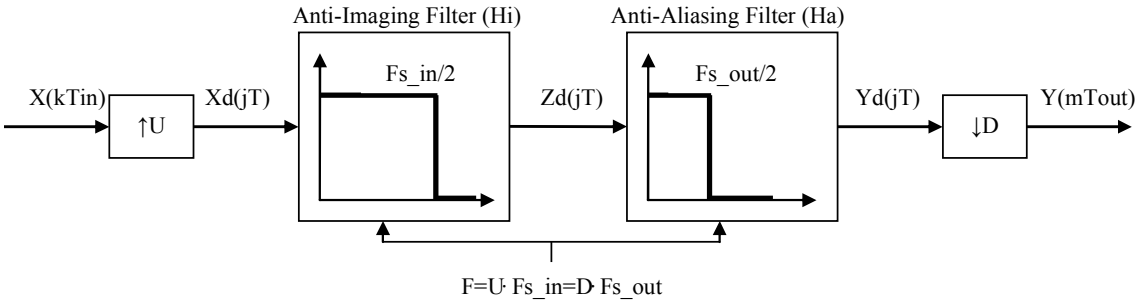

Figure 6. All-digital solution for the SRC.

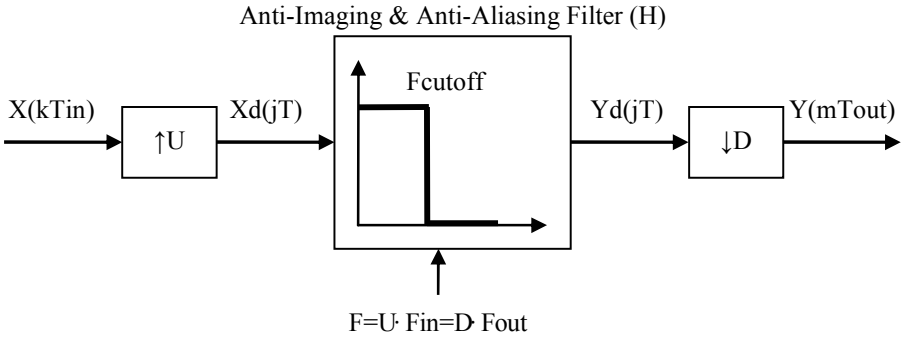

Figure 7. Optimized all-digital solution for SRC.

The ideal transfer function of the digital filter is given by:

$$H(f)=\begin{cases}U, & \text{if } 0<f<\min(Fs\_in/2, Fs\_out/2)\\ 0, & \text{if } \min(Fs\_in/2, Fs\_out/2)<f<F/2\end{cases} \quad (3)$$

Although the digital-domain solution enables one to forget the detour via reconstructing an analog signal and re-sampling it, it's very important to always keep in mind that SRC is a process of re-sampling.

The basic equations describing the signal processing involved can be derived from the diagram above, resulting in a digital-domain description of the necessary filtering task. First step is the up-sampling:

$$Xd(jT)=\begin{cases}X(kTin), & \text{if } j=kU \text{ with } k=0,\pm1,\pm2,...\\ 0, & \text{otherwise}\end{cases} \quad (4)$$

The multiplication of a signal with spectrum Xd(f) by a transfer function H(f) in frequency domain leads to the signal Yd(f)=H(f)·X(f), which corresponds to a convolution of the signals in the discrete-time domain:

$$\begin{aligned} &Yd(jT)=Xd(jT)*H(jT)\\ &\qquad\Updownarrow\\ &Yd(jT)=\sum_{-\infty}^{+\infty}Xd(iT)H((j-i)T)\end{aligned} \quad (5)$$

Since Xd(jT) is the up-sampled (zero padded) version of X(kTin) and many values are equal to zero, the last equation can be simplified a bit:

$$Yd(jT)=\sum Xd(iT)\cdot H((j-i)T), \quad \text{with } i=0,\pm U,\pm 2\cdot U,... \quad (6)$$

The final signal after the down-sampling process is described by:

$$Y(mTout)=Yd(jT), \text{if } j=mD \quad \text{with } m=0,\pm1,\pm2,... \quad (7)$$

C. SRC and CIC Filtering

Since power consumption is a major issue in mobile communications systems, at least in the mobile terminal side, hardware structures that implement the necessary filtering tasks efficiently are sought. Moreover, these hardware structures should be adaptive in such a way that SRC can be performed independent of the current standard of operation. One efficient way of implementing them was first proposed by Hogenauer [3], under the name of Cascaded Integrator Comb filters, or CIC filters [4]. Their major advantage is the very efficient architecture making them very suitable in the case of digital hardware implementations.

The CIC filter has two major sections: a comb section, which is a cascade of *N* combs, and an integrator section, which is a cascade of *N* integrators. The two sections are separated by an expander, with an expansion ratio *R*. The expander could be an up-sampling unit or a down-sampling unit. In general, the system sample rate is much higher than the bandwidth occupied by the signal.

1) CIC Decimator

Figure 8 shows the basic structure of the one stage CIC decimation filter. It consists of one integrator followed by a down-sample block and one comb filter.

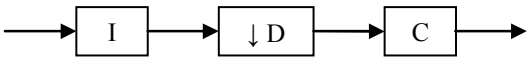

Figure 8. First order CIC decimator.

The integrator section is operating at high sampling rate and it is implemented as one-pole IIR filter with a unity feedback coefficient (Figure 9):

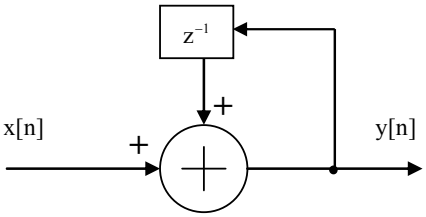

Figure 9. Digital Integrator (or Accumulator).

The equation describing this block is:

$$y[n]=y[n-1]+x[n] \quad (8)$$

The system is also known as an accumulator and its transfer function in the z-domain is:

$$Hi(z)=\frac{1}{1-z^{-1}} \quad (9)$$

The power response is basically a low-pass filter with 20 dB per decade roll-off, but with infinity gain at DC. This is due to the single pole at z=1. Therefore the output can grow without bound for a bounded input, making the system unstable.

The structure of the comb filter after the down-sampling unit is described by the following diagram (Figure 10):

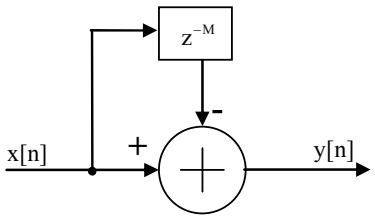

Figure 10. First order comb filter.

The equation describing this block is:

$$y[n]=x[n]-x[n-M] \quad (10)$$

M is a design parameter called differential delay used to control the filter frequency response. *M* can be any positive integer, but it is usually limited to 1 or 2 (when it is 1, the block becomes a classic differentiator). By using multi-rate digital signal techniques (Noble's identities) [5], the comb filter can be "pushed" in front of the down-sample block, thus becoming a comb filter operating at the same frequency as the integrator, but described by a different equation:

$$y[n]=x[n]-x[n-DM] \quad (11)$$

where *D* is the down-sampling value. The corresponding transfer function in the z-domain is:

$$Hc(z)=1-z^{-DM} \quad (12)$$

The composite frequency response of the integrator and the comb filter (*M*=1), referenced to the frequency after the down-sampling block, is:

$$H(z) = Hi(z) \cdot Hc(z)$$
$$H(z) = \frac{1 - z^{-D}}{1 - z^{-1}} \Leftrightarrow H(z) = \sum_{k=0}^{D-1} z^{-k} \quad (13)$$

As mentioned before, the down-sampling unit can be placed at the end and, thus, we obtain the equivalent diagram of the CIC decimator, with *H(z)* being the function described above (Figure 11):

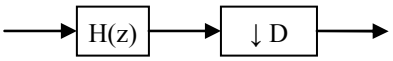

Figure 11. Equivalent structure for the CIC decimator.

Following the same procedure, it can be shown that the equivalent transfer function for the general CIC decimator made from N stages (N cascaded integrators instead of one and N cascaded comb filters instead of one) is:

$$H(z) = \left[\frac{1 - z^{-D}}{1 - z^{-1}}\right]^N \Leftrightarrow H(z) = \left[\sum_{k=0}^{D-1} z^{-k}\right]^N \quad (14)$$

Evaluating this equation at $z = e^{j \cdot 2\pi f}$ we get the equivalent transfer function in the normalized frequency domain:

$$|H(f)|^2 = \left[\frac{1 - \cos(2\pi fD)}{1 - \cos(2\pi f)}\right]^N \Leftrightarrow$$
$$|H(f)| = \left[\frac{\sin(\pi fD)}{\sin(\pi f)}\right]^N \quad (15)$$

2) CIC Interpolator

Interchanging the integrator with the comb filter and replacing the down-sampler with an up-sampler produces the CIC interpolator (Figure 12):

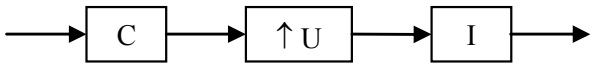

Figure 12. First order CIC interpolator.

The comb filter is described by the same equation like (9):

$$y[n] = x[n] - x[n - UM]$$

and again we will use a multi-rate digital signal processing technique to "push" this time the up-sampling block in front of the comb filter. The resulted equation will be:

$$y[n] = x[n] - x[n - UM] \quad (16)$$

with the equivalent transfer function in the z-domain:

$$Hc(z) = 1 - z^{-UM} \quad (17)$$

The integrator keeps the same transfer function in the z-domain (9):

$$Hi(z) = \frac{1}{1 - z^{-1}}$$

The composite frequency response of the comb filter (M=1) and the integrator, referenced to the frequency after the up-sampling block, is:

$$H(z) = Hc(z) \cdot Hi(z)$$
$$H(z) = \frac{1 - z^{-U}}{1 - z^{-1}} \Leftrightarrow H(z) = \sum_{k=0}^{U-1} z^{-k} \quad (18)$$

The equivalent diagram of the CIC interpolator using the above transfer function is shown below (Figure 13):

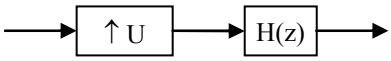

Figure 13. Equivalent structure for the CIC interpolator.

The equivalent transfer function in the normalized frequency domain is very similar to the one of the decimator:

$$|H(f)|^2 = \left[\frac{1 - \cos(2\pi fU)}{1 - \cos(2\pi f)}\right]^N \Leftrightarrow$$
$$|H(f)| = \left[\frac{\sin(\pi fU)}{\sin(\pi f)}\right]^N \quad (19)$$

By notating with *R* the change rate of either a CIC decimator or CIC interpolator, the equation describing the transfer function in the z-domain and normalized frequency domain takes the general form:

$$H(z) = \left[\sum_{k=0}^{R-1} z^{-k}\right]^N \quad (20)$$

$$|H(f)| = \left[\frac{\sin(\pi f \cdot R)}{\sin(\pi f)}\right]^N \quad (21)$$

The CIC filter is equivalent to a cascade of *N* uniform FIR filter stages with unity coefficients. These filters are also known under the name of box-car filters or moving average filters. Their transfer function has a low-pass frequency characteristic with nulls (transfer function zeros) at integer multiples of f=1/R.

One observation to be made at this stage is that, generally, the "sinc" name is associated with the transfer function of these filters. The basis for that is the fact that for very small values of f, sin(πf) can be approximated with πf, but keep in that the real transfer function is (20).

3) CIC – Frequency Responses

The CIC frequency responses to various orders were depicted in Figure 14.

The transfer function has a low-pass frequency characteristic with nulls (transfer function zeros) at integer multiples of f=1/R. The frequency response graph is showing that the attenuation of the CIC filter increases with *N*. A more precise formula on how this attenuation is related to N is provided below:

$$H2(f) = \frac{N2}{N1} \cdot H1(f) \quad (22)$$

The *H*1(*f*) is the transfer function of the CIC filter with *N*1 stages, and *H*2(*f*) is the transfer function of the same type of CIC filter, but with *N*2 stages. Both transfer functions should be expressed in dB.

In other words, the attenuation is directly proportional with the number of stages. For example, if the attenuation at the frequency fa, using *N*1=1 stage is –20 dB, by using *N*2=2 stages we will get an attenuation at fa of –40 dB and by using *N*3=3 stages we get –60 dB attenuation (Figure 15).

In general, the band of interest for the signal at the input of the CIC filter is less than 1/8 from the available bandwidth (Fs/2) in order to make these filters efficient in

eliminating the images or preventing aliasing.

The smaller is the band of interest, the better is the rejection of images or the aliasing frequencies, therefore, the worst case for an image/alias rejection Fig. for a signal will be when the signal frequency is at the end of the available bandwidth.

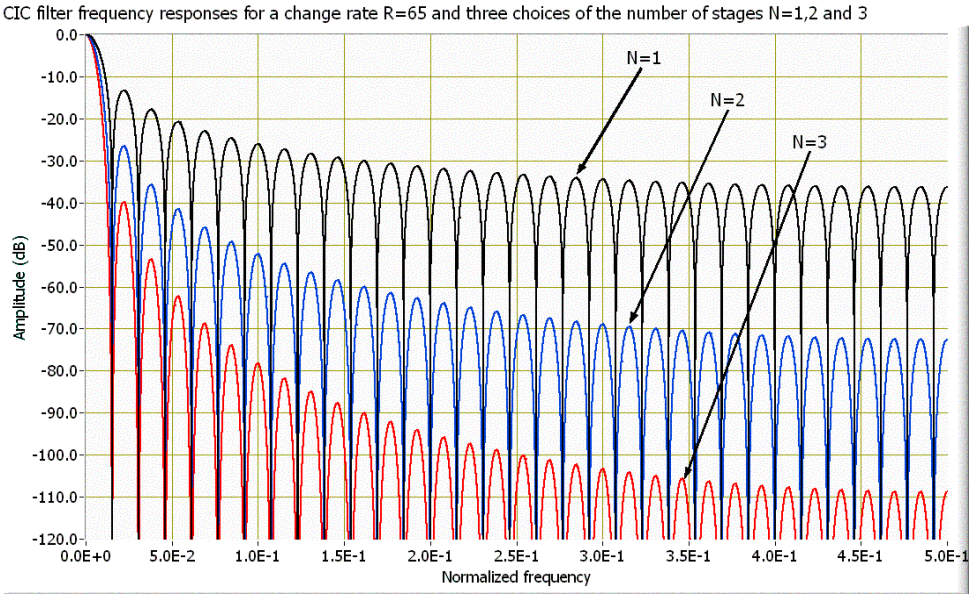

Figure 14. Frequency responses for CIC filters of orders 1, 2 and 3.

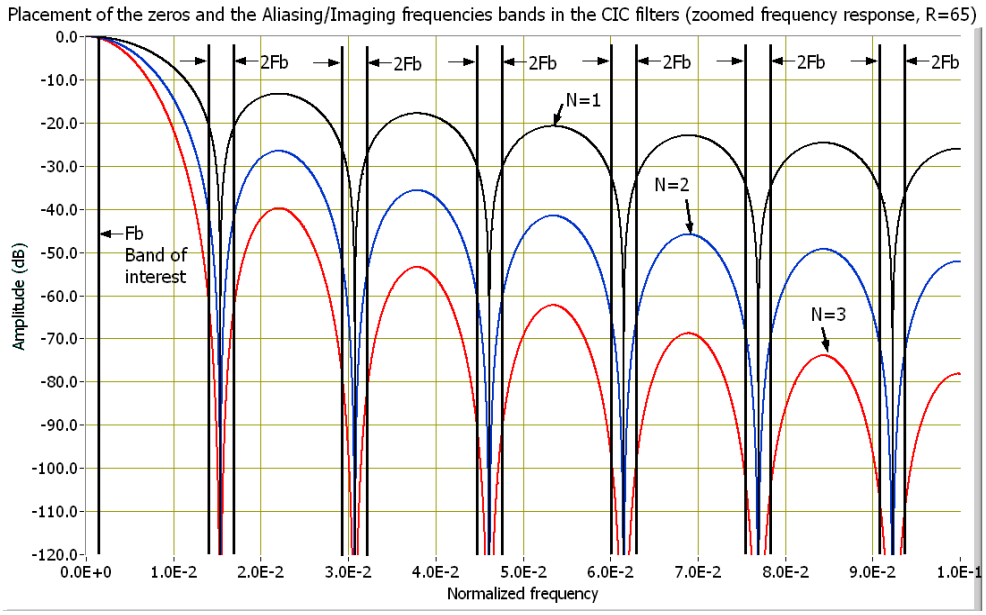

Figure 15. Zoomed version of Frequency responses for CIC filters.

Below is the formula for the location of Aliasing/Imaging frequencies bands, in the normalized frequency domain (referenced to the high frequency):

$$\left(\frac{k}{R}-Fb,\frac{k}{R}+Fb\right), \text{ with } k=1,2,3,\ldots,[R/2] \tag{23}$$

Fb is the band of interest (in general is 1/ (2·8·R)) (Figure 16).

It can be seen that the attenuation in the band of interest increases with *N* and, therefore, when increasing *N* to obtain a better rejection of the aliases/images, we must keep in mind the effect of that to the signals in the band of interest.

Another observation refers to the ratio between the band of interest and the sampling rate: the smaller is it, the less attenuation in the band of interest occurs.

IV. CONCLUSIONS

This paper presents basic consideration needed to understand the challenges of incorporating more and more functionality (for example, "audio + intermediate radio frequency") into a single IC (integrated circuit); coming up with SoC (System on Chip) is a necessity these days when more and more electronic devices are becoming mobile.

Based on these considerations several solutions that allow this high level of integration will be explored and, for each one, the main implementation difficulties will be outlined.

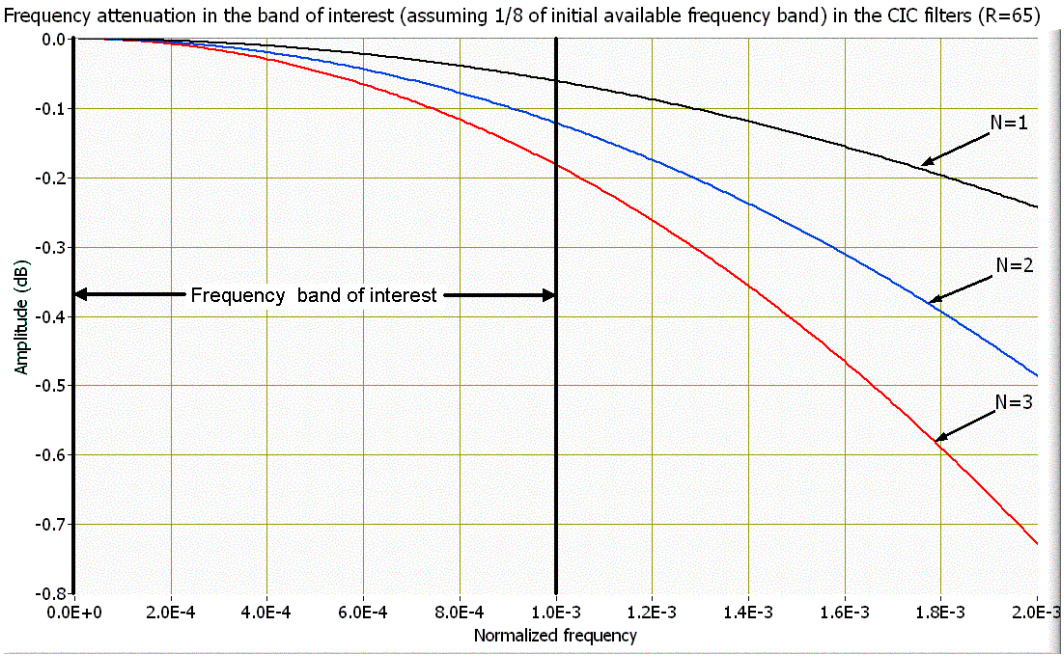

Figure 16. Frequency attenuation in the band of interest for CIC filters.

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