A VLSI Implementation of a New Low Voltage 5th Order Differential G_m-C Low-Pass Filter with Auto-Tuning Loop in CMOS Technology

Radu Gabriel BOZOMITU, Neculai COJAN
Faculty of Electronics, Telecommunications and Information Technology,
"Gh. Asachi" Technical University, Carol I No.11 Av., 700506, Iaşi, Romania
bozomitu@etti.tuiasi.ro, ncojan@etti.tuiasi.ro

***Abstract*—In this paper a new low voltage 5th order G_m-C Bessel type low-pass filter (LPF) with auto-tuning loop and higher dynamic range, designed in CMOS technology, is presented. The cut-off frequency can be tuned in (10 – 42)MHz range by modifying the values of the grounded capacitors using a digital logic. The proposed structure is based on an auto-tuning loop in order to maintain the G_m/C ratio independent of the process, supply voltage and temperature variations, assuring the cut-off frequency of the LPF independently of these factors. The proposed 5th order G_m-C Bessel type low-pass filter provides a ±5% variation of the cut-off frequency in all critical corners, a 400mV$_{pp(diff)}$ dynamic range, THD < 1% and 21.6mW power consumption from 1.8V supply voltage. The simulations performed in 65nm CMOS process confirm the theoretical results.**

***Index Terms*— auto-tuning, biquad, CMOS, G_m-C filter, transconductor, VLSI.**

I. Introduction

G_m-C filters are the most popular technique used in implementing integrated high frequency continuous-time (CT) filters [1] – [17]. Most CT filters contain integrators as basic building blocks. Their popularity is given by the fact that transconductors are very easy to implement in monolithic form; they also have a higher bandwidth than operational amplifiers, can be tuned electronically and lead to simple circuitry [1] – [17].

One of the main problems that occur in active filters designing is represented by the fact that the cut-off or centre frequencies are strongly depending on the process, temperature and supply voltage variations [1] – [11].

Another important problem reported in literature is represented by the narrow dynamic range of the input signal for which the circuit works linearly [12] – [16].

In this paper a new low voltage 5th order differential ***G_m-C*** Bessel type low-pass filter (LPF) with auto-tuning loop and higher dynamic range, which solves the above constraints, has been designed in CMOS technology.

Unlike other ***G_m-C*** techniques reported in the literature, based on constant-G_m biasing or others [1] – [4], [17] the proposed solution presented in this paper uses an auto-tuning loop, which provides the bias currents (used in ***G_m-C*** filter core), keeping the ***G_m/C*** ratio independent of the process, supply voltage and temperature variations. This is a very important aspect, considering that the capacitors used in the proposed LPF implementation are strongly depending on these variations.

The paper is organized as follows. In Section II, the proposed filter topology is presented and analyzed by simulations at the system level. Bode characteristics of the ideal 5th order differential Bessel type LPF are shown. In Section III is presented the proposed transconductor cell with higher dynamic range, which is used in 5th order differential Bessel type LPF implementation. In Section IV, the proposed tuning loop architecture designed to maintain the ***G_m/C*** ratio independent of the process, supply voltage and temperature variations, is presented. The operation of the proposed structure is presented in Section V by simulations in 65nm CMOS technology. A few conclusions of this paper are illustrated in Section VI.

II. Topology of the 5th Order Differential Gm-C Bessel Type Low-Pass Filter with Auto-Tuning Loop

In Fig. 1 the block diagram of the proposed structure is shown. The 5th order differential ***G_m-C*** Bessel type LPF with auto-tuning loop is composed by a 5th order differential ***G_m-C*** LPF core, an auto-tuning loop used to generate the bias currents keeping constant the ***G_m/C*** ratio (independent of the process, supply voltage and temperature variations), and an external differential no-overlap clock (NOVCK) of 50MHz.

In general, the cut-off frequency of a ***G_m-C*** filter can be tuned by using external bias currents or modifying the values of the grounded capacitors. Since the proposed structure illustrated in Fig. 1 uses the bias currents provided by the auto-tuning loop, the second variant of cut-off frequency tuning is preferred.

Thus, the cut-off frequency of the proposed LPF can be

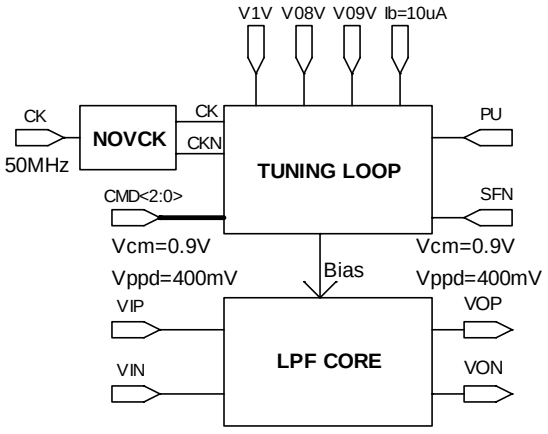

Figure 1. Block diagram of the LPF with auto-tuning

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tuned in (10 – 42)MHz range, by using digital command logic, according to three control bits, noted CMD<2:0> in Fig. 1.

The 5th order differential G_m-C Bessel type low-pass filter in Fig. 1 is designed so that it can operate with constant bias currents, too. Thus, the proposed structure shown in Fig. 1 provides two operation modes, according to the value of SFN control bit, illustrated in Fig. 1: a) first operation mode (SFN = 0) – bias currents are provided by the auto-tuning loop, keeping constant the G_m/C ratio; b) second operation mode (SFN = 1) – constant bias currents. In this operation mode, the cut-off frequency of the LPF can be tuned by modifying the external bias currents. Both operation modes will be analyzed and compared in next sections in this paper.

In Fig. 2, the block diagram of the 5th order differential G_m-C Bessel type low-pass filter core is shown. This is composed of two biquad structures and a first order low-pass filter [17].

To obtain the 42MHz cut-off frequency, the poles of the 5th order differential LPF in Bessel approximation need to have the values in Table 1.

TABLE 1. POLES OF THE 5TH ORDER DIFFERENTIAL LPF IN BESSEL APPROXIMATION FOR 42MHZ CUT-OFF FREQUENCY

Filter type	Bessel
Cut-off frequency (MHz)	42
DC gain	1
Real pole*	-392.270
Intermediate poles*	-360.561±j·187.453
HF poles*	-250.059±j·384.126

***(x10^6 rad/s)**

The Bode characteristics of the ideal 5th order, Bessel type LPF, for a cut-off frequency of 42MHz are illustrated in Fig. 3. From Fig. 2, the transfer function of the 5th order differential G_m-C Bessel type low-pass filter can be written [17]:

$$H(s)=\frac{G_m^2/(C_1C_2)}{s^2+s\frac{G_m}{C_2}+\frac{G_m^2}{C_1C_2}}\cdot\frac{G_m^2/(C_3C_4)}{s^2+s\frac{G_m}{C_4}+\frac{G_m^2}{C_3C_4}}\cdot\frac{G_m/C_5}{s+\frac{G_m}{C_5}} \quad (1)$$

According to equation (1), the 5th order differential G_m-C Bessel type low-pass filter has 5 the poles, denoted as follows:

$$p_{1,2}=\alpha_1\pm j\beta_1,\ p_{3,4}=\alpha_2\pm j\beta_2,\ p_5=\alpha_3 \quad (2)$$

Using the poles values in Bessel approximation, given by Table 1 and noted as equations (2) show, in the denominator of LPF transfer function from equation (1), then by terms identification, the grounded capacitor values can be obtained [17]:

$$\begin{cases} C_1=-\dfrac{2\alpha_1\cdot G_m}{\alpha_1^2+\beta_1^2};\ C_2=-\dfrac{G_m}{2\alpha_1};\\ C_3=-\dfrac{2\alpha_2\cdot G_m}{\alpha_2^2+\beta_2^2};\ C_4=-\dfrac{G_m}{2\alpha_2};\ C_5=-\dfrac{G_m}{\alpha_3} \end{cases} \quad (3)$$

Knowing the poles values of the 5th order differential G_m-C LPF in Bessel approximation, given by (α_1, β_1), (α_2, β_2) and α_3 in equations (2), and choosing an appropriate value for differential transconductance G_m in Fig. 2 (i.e. $G_m = 0.9\text{mS}$), the values of the grounded capacitors which determine a 42MHz cut-off frequency are presented in Table 2. The used capacitors (implemented on the base of nMOS transistors in nwell process) are provided by technology. Their capacitance value depends on the aspect ratio (W/L) of the nMOS transistors [17].

TABLE 2. GROUNDED CAPACITORS DEPENDING ON CUT-OFF FREQUENCY OF THE 5TH ORDER DIFFERENTIAL G_m-C BESSEL TYPE LPF

C / Freq	C_1 [pF]	C_2 [pF]	C_3 [pF]	C_4 [pF]	C_5 [pF]
42 MHz	4	1.27	2.19	1.84	2.34

The G_m transconductor shown in block diagram from Fig. 2 is implemented using a differential operational transconductance amplifier (OTA) designed for an extended dynamic range linear operation. In Section III, the complete analysis of this circuit is presented.

In order to maintain the cut-off frequency of the proposed LPF independent of the process, supply voltage and temperature variations, the bias currents used by the analyzed structure are provided by the auto-tuning loop, which keeps constant the G_m/C ratio in all critical corners. In Section IV, the design of this auto-tuning loop is presented.

III. IMPLEMENTATION OF THE G_m TRANSCONDUCTOR AT THE CIRCUIT LEVEL

In Fig. 4 the electric scheme of the G_m transconductor used in LPF core is presented.

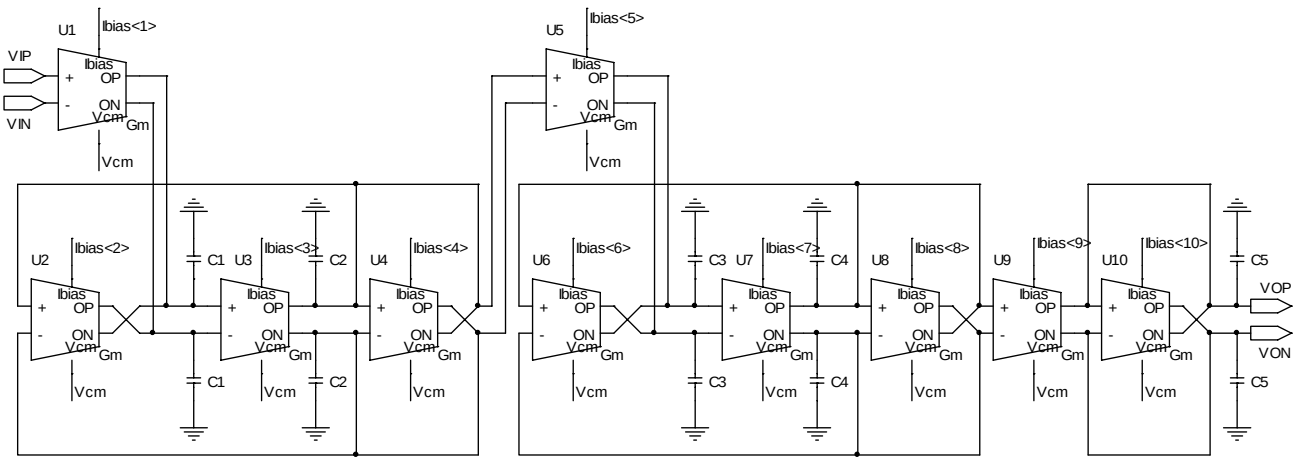

Figure 2. Block diagram of 5th order G_m-C Bessel type low-pass filter core

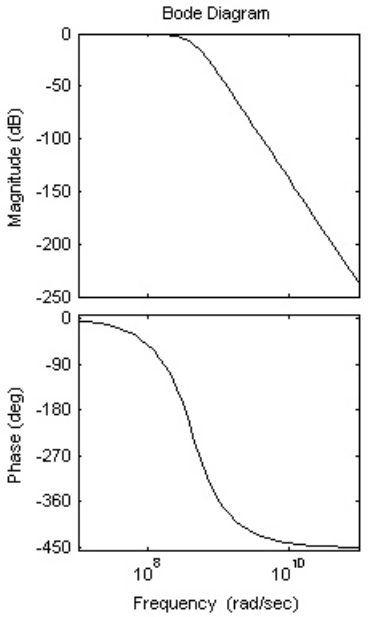

Figure 3. Bode characteristics of the ideal 5th order Bessel type LPF for a cut-off frequency of 42 MHz

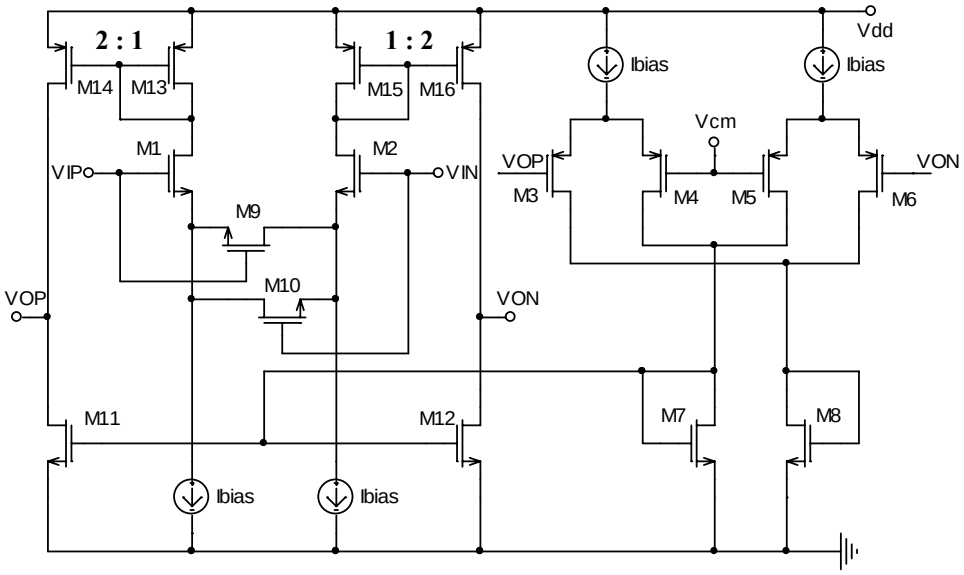

Figure 4. Electric scheme of the transconductor from G_m-C filter

The proposed $\boldsymbol{G_m}$ cell in Fig. 4 is formed by a differential pair implemented with M_1 and M_2 transistors and a common mode feedback (CMFB) loop represented by M_3 – M_8 transistors.

The linearity of the proposed transconductor can be sensibly improved by using a topology with M_9 and M_{10} transistors [5].

For the circuit illustrated in Fig. 4, the classic resistive degeneration has been replaced by MOSFET transistors M_9 and M_{10} operating in deep triode region.

For this structure, M_9 and M_{10} are in deep triode region if $\boldsymbol{V_{in} = 0}$. As the gate voltage of M_1 becomes more positive than the gate voltage of M_2, transistor M_9 stays in the triode region because $\boldsymbol{V_{D9} = V_{G9} - V_{GS1}}$ whereas M_{10} eventually enters the saturation region because its drain voltage rises and its gate and source voltage fall [5].

Thus, the circuit remains relatively linear even if one degeneration device goes into saturation.

For the widest linear region it is suggested in [9] that:

$$\left(\frac{W}{L}\right)_{1,2} \approx 7\left(\frac{W}{L}\right)_{9,10} \tag{4}$$

If we note with $\boldsymbol{R_{lin}}$ the equivalent linearization resistor given by M_9 and M_{10} transistors which operates in triode region, then the differential transconductance value of the circuit illustrated in Fig. 4 can be written:

$$G_m = \frac{4g_m}{2 + g_m \cdot R_{lin}} \tag{5}$$

where $\boldsymbol{g_m}$ is the transconuctance value of the each transistor which forms the differential input pair, given by

$$g_m = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)_{1,2} I_{bias}} \tag{6}$$

and the expression of the linearization resistor is:

$$R_{lin} = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)_{9,10}\left(V_{GS(9,10)} - V_{TH}\right)} \tag{7}$$

For many applications, the value of the linearization resistor, $\boldsymbol{R_{lin}}$, is smaller than the inverse of the circuit transconductance, $\boldsymbol{g_m}$:

$$R_{lin} << 1/g_m \tag{8}$$

If condition (8), is fulfilled, than from (5) the differential transconductance value can be approximated as:

$$G_m \approx 2g_m \tag{9}$$

In order to obtain the 5th order differential G_m-C Bessel type LPF parameters, imposed by design conditions, a precise value of the $\boldsymbol{G_m}$ from Fig. 4 is needed in equations (3).

The value of the $\boldsymbol{G_m}$ can be calculated by using the test scheme illustrated in Fig. 5. In the following, the operation of this test circuit is presented.

Both cells from test circuit shown in Fig. 5 are identical, having the differential transconductances values noted $\boldsymbol{G_m}$. The second cell in Fig. 5 operates as an equivalent differential resistor $\boldsymbol{R}$, having the absolute resistance given by:

$$R = 1/G_m \tag{10}$$

The differential output currents provided by the two transconductors in Fig. 5 can be written:

$$I^+_{out1} - I^-_{out1} = G_{m1} \cdot \Delta V_{in}\,; \quad I^+_{out2} - I^-_{out2} = -G_{m2} \cdot \Delta V_{out} \tag{11}$$

where $\boldsymbol{G_{m1}}$ and $\boldsymbol{G_{m2}}$ are the differential transconductance values of the two cell, respectively and

$$\Delta V_{in} = V^+_{in} - V^-_{in}\,; \quad \Delta V_{out} = V^+_{out} - V^-_{out} \tag{12}$$

If we neglect the output resistances of the transconductor cells, $\boldsymbol{R_{out}}$ ($\boldsymbol{R_{out} >> 1/G_m}$) for the test circuit in Fig. 5 one can write the following equations:

$$\begin{cases} I^+_{out1} + I^-_{out2} = 0 \\ I^-_{out1} + I^+_{out2} = 0 \end{cases} \tag{13}$$

By using equations (11) in (13) we obtain:

$$\frac{\Delta V_{out}}{\Delta V_{in}} = -\frac{G_{m1}}{G_{m2}} \tag{14}$$

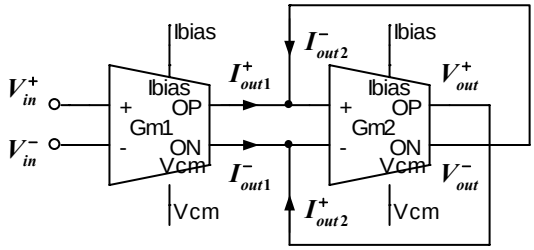

Figure 5. Test circuit to calculate the transconductance value, G_m

Thus, for a perfect matching between the two cells ($G_{m1} = G_{m2} = G_m$), the test circuit in Fig. 5 operates as an ideal voltage inverter and from (14) the following equation can be written:

$$A_v = \Delta V_{out} / \Delta V_{in} = -1 \tag{15}$$

If the condition $R_{out} >> 1/G_m$ is fulfilled for the G_m cells in the test scheme illustrated in Fig. 5, then this circuit can be used in order to precisely evaluate the differential transconductance value, G_m.

Thus, using the circuit illustrated in Fig. 5, the differential transconductance value, G_m, can be obtained from equation (11) as follows:

$$G_m = \frac{I_{out1}^+ - I_{out1}^-}{V_{in}^+ - V_{in}^-} \tag{16}$$

In Section V, the calculation of the differential transconductance value, according to equation (16), will be illustrated by simulation in a 65nm CMOS technology.

IV. Auto-Tuning Loop Design

The principle of the auto-tuning loop can be explained by using the block scheme shown in Fig. 6.

The proposed auto-tuning loop provides the bias currents used in 5th order differential G_m-C Bessel type LPF core, keeping the G_m/**C** ratio independent of the process, supply voltage and temperature variations. Since the cut-off frequency of the G_m-C filters depend on G_m/**C** ratio, using this technique we can maintain the cut-off frequency of the proposed LPF, independently of these variations.

The auto-tuning loop shown in Fig. 6 is composed by a transconductor cell ($G_{m\_replica}$), which represents a replica of the transconductor cells used in LPF core from Fig. 2, a double differential operational amplifier (OPAMP) providing the output in current and two fixed resistors R_{S1} and R_{S2}. In order to be independent of the process, supply voltage and temperature variations, the two fixed resistors shown in Fig. 6 are replaced by a switched-capacitor equivalent [5], [16]. In order to implement these two switched-capacitor equivalent resistors an external clock of 50MHz is used.

The value of the equivalent resistor on the branch, $R_S = R_{S1} = R_{S2}$ is given by the following equation [5]:

$$R_S = \frac{1}{f_{ck} C_S} \tag{17}$$

where f_{ck} denotes the clock frequency and $C_S = C_{S1} = C_{S2}$ is the total capacitance on the branch. Capacitors C_{f1} and C_{f2} are added to shunt the high-frequency components resulting from switching to ground. Since the absolute value of the capacitor is typically more tightly controlled and since the temperature coefficient (TC) of capacitors is much smaller than that of resistors, this technique provides a higher reproducibility in the bias current and transconductance [5].

The input voltages of the G_m replica ($G_{m\_replica}$) are represented by two fixed voltages denoted V_1 and V_2, respectively, in the block scheme from Fig. 6.

The values of these voltages are: $V_1 = 1$**V** and $V_2 = 0.8$**V**. The common mode voltage of the G_m transconductor cell is $V_{cm} = 0.9$**V**.

The differential output current provided by the G_m replica from Fig. 6 can be written:

$$i_{Gm} = G_m \cdot v_{i(REF)} \tag{18}$$

where

$$v_{i(REF)} = V_1 - V_2 = 200\text{mV} \tag{19}$$

and $i_{Gm} = i_{Gm}^+ - i_{Gm}^-$ represents the differential output current provided by the G_m replica transconductor.

The bias current of the G_m replica (I_{bias}**<10>** in Fig. 6) is given by the loop. The other 10 replicas of this current (I_{bias}**<9:0>**) are used as bias currents for each G_m transconductor cells of LPF core from Fig. 2.

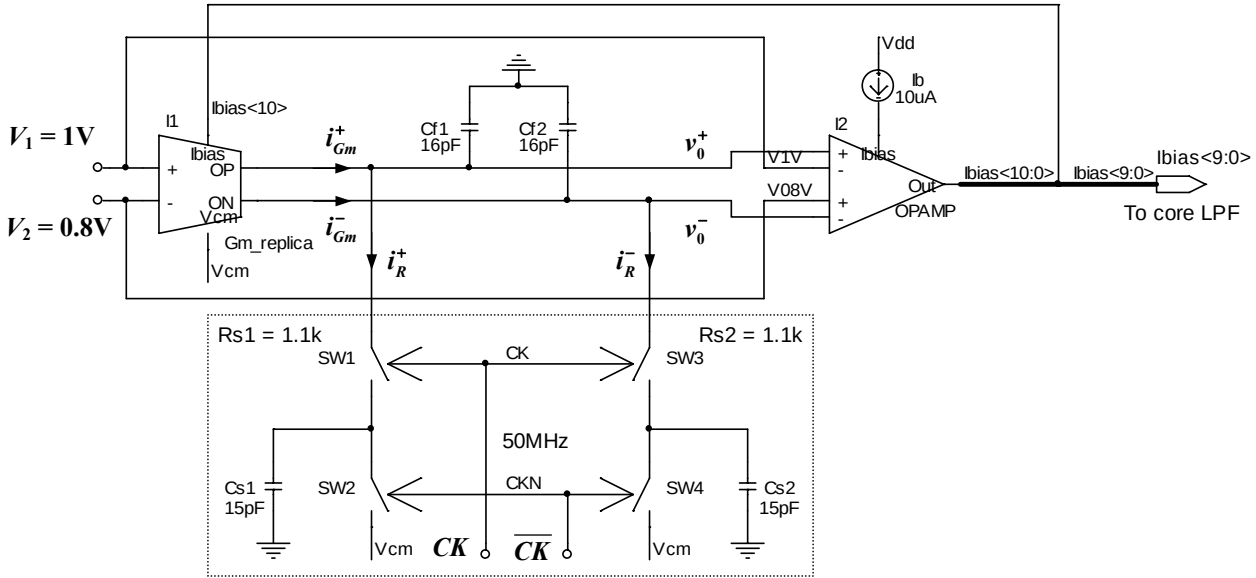

Figure 6. Block scheme of the auto-tuning loop used in 5th order differential G_m-C Bessel type LPF implementation

The differential current through the switched-capacitor equivalent resistors can be written:

$$i_R = v_0 / R_S \quad (20)$$

where

$$i_R = i_R^+ - i_R^-;\ v_0 = v_0^+ - v_0^- \quad (21)$$

In equation (20), R_S represents the switched-capacitor equivalent resistor, given by equation (17).

For a high input impedance of the OPAMP, from Fig. 6 is evident that the differential output current provided by the G_m replica transconductor (i_{Gm}) is the same with the differential current through the switched-capacitor equivalent resistor, i_R.

On the other hand, the loop assures that the differential voltage on the switched-capacitor equivalent resistors, ($v_0 = v_0^+ - v_0^-$) is equal to the difference between the two reference voltages V_1 and V_2, used as reference voltages at the other two inputs, respectively, of the double differential OPAMP from Fig. 6. This voltages difference has been expressed by the equation (19).

Taken into consideration the above observations, the following equations can be written:

$$\begin{cases} i_{Gm} = i_R \\ v_0 = v_{i(REF)} \end{cases} \quad (22)$$

Using equations (18) and (20) in first equation (22), and taken into consideration the second equation (22) we obtain:

$$G_m = 1 / R_S \quad (23)$$

The second equation (22) is fulfilled by the auto-tuning loop. Thus, by using this feedback mechanism, the bias current provided by the loop (I_{bias}**<10>**) has a value so that, the G_m replica transconductance is equal with the inverse of the switched-capacitor equivalent resistor, R_S, as equation (23) shows.

According to equation (23), and taken into consideration that the transconductance value to accomplish the design conditions is $G_m = 0.9\text{mS}$, for optimal operation of the auto-tuning loop from Fig. 6, a switched-capacitor equivalent resistor having the value $R_S = 1/G_m = 1.1\text{k}\Omega$ is needed. For this resistor value and using a clock frequency $f_{ck} = 50\text{MHz}$, according to equation (17), the value of the C_S capacitor is **18pF**.

Using (17) in equation (23), we obtain the following constant value for the G_m/C_s ratio:

$$G_m / C_s = f_{ck} \quad (24)$$

In order to diminish the high frequency ripple of 50MHz introduce by switched-capacitor equivalent resistors (chosen higher than maximum cut-off frequency of the proposed LPF), two filtering capacitors C_{f1} and C_{f2} are used in the auto-tuning loop presented in Fig. 6.

The filtering capacitors determine the increase of the C_S capacitor value, and consequently, according to (24), the value of the G_m transconductor will be increased, too. In order to maintain the transconductance value G_m around the value of **0.9mS** (resulted by design conditions), the value of C_S capacitor must be diminished from 18pF.

According to these considerations, the optimal values of capacitors shown in auto-tuning loop in Fig. 6 are: $C_{S1} = C_{S2} = 15\text{pF}$ and $C_{f1} = C_{f2} = 16\text{pF}$.

So, by using this technique, illustrated in Fig. 6, we can provide bias currents keeping the G_m/C_s ratio independent of the process, supply voltage and temperature variations, according to equation (24).

Since these bias currents are used in the LPF core from Fig. 2, results that the cut-off frequency of the proposed structure will be independent of these variations.

In order to demonstrate and validate this result, in Section V we compare by simulation in 65nm CMOS technology the behavior of the proposed 5th order differential G_m-C Bessel type LPF for the two operation modes: with constant bias currents and with the bias currents provided by the auto-tuning loop.

V. Simulations Results

The operation of the proposed 5th order differential G_m-C Bessel type low-pass filter with auto-tuning loop is analyzed by simulation in different critical corners in order to show that its cut-off frequency is independent of the process, supply voltage and temperature variations.

The proposed circuit has been analyzed by simulation in a 65nm CMOS technology by using an input signal of $400\text{mV}_{pp(diff)}$ and 1.8V supply voltage.

First, in order to calculate the transconductance value of the G_m cell shown in Fig. 4, the test circuit from Fig. 5 is analyzed by simulation in 65nm CMOS technology.

In Fig. 7 the DC differential output currents depending on the input voltage of the G_m, for a unitary voltage gain and for $I_{bias} = (60 \div 120)\mu\text{A}$ are shown.

In Fig. 8 the differential transconductances depending on the input voltage for a unitary voltage gain and for $I_{bias} = (60 \div 120)\mu\text{A}$ are presented. From this DC simulation, a desired value of the differential transconductance can be obtained for $I_{bias} = (70 - 80)\mu\text{A}$ and the dynamic range of the input signal for which the circuit operates linearly is about $400\text{mV}_{pp(diff)}$. The dynamic range represents the range values of the input signal for which the transconductance value is constant and independent of the input voltage with an error $\varepsilon \le 1\%$.

In Fig. 9 the differential voltage gains depending on the input voltage of the G_m for $I_{bias}=(60 \div 120)\mu\text{A}$ are presented. From this simulation, a value of DC gain of 0.95 is obtained. The difference to unitary voltage gain is due to finite output resistance of the proposed G_m cell.

In Fig. 10 the AC frequency responses of the G_m in closed loop operation (unitary voltage gain) for $I_{bias} = (60 \div 120)\mu\text{A}$ are shown. The cut-off frequency is about 700MHz.

In Fig. 11 the AC frequency response of the G_m in open loop for $I_{bias}=80\mu\text{A}$ is presented. The gain of the proposed transconductor is about 32dB.

Next, the transient simulations of the proposed 5th order differential G_m-C Bessel type low-pass filter with auto-tuning loop from Fig. 1 are performed in all critical corners in order to determine the bias currents values, depending on the process, supply voltage and temperature variations. These bias currents are presented in Fig. 12 and their values depending on the corners are shown in Table 3.

In Fig. 13 the differential output voltage (VOP-VON) of the proposed LPF in Fig. 1, depending on corners, for a 42MHz input signal with $400\text{mV}_{pp(diff)}$ magnitude, is presented; a very small variation of these waveforms results.

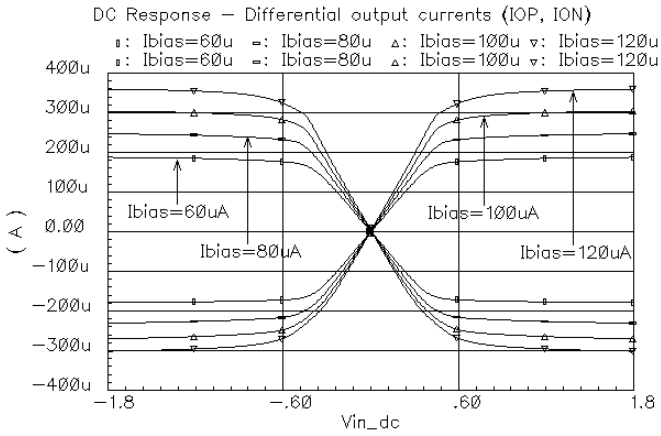

Figure 7. Differential output currents provided by the test circuit from Fig. 5 for different values of the bias current (**I_{bias} = (60 ÷ 120)µA**)

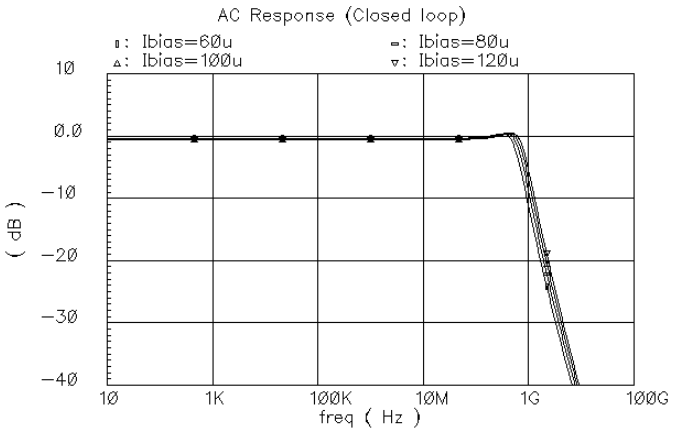

Figure 10. Small signal frequency response of the G_m in closed loop for different values of the bias current (**I_{bias} = (60 ÷ 120)µA**)

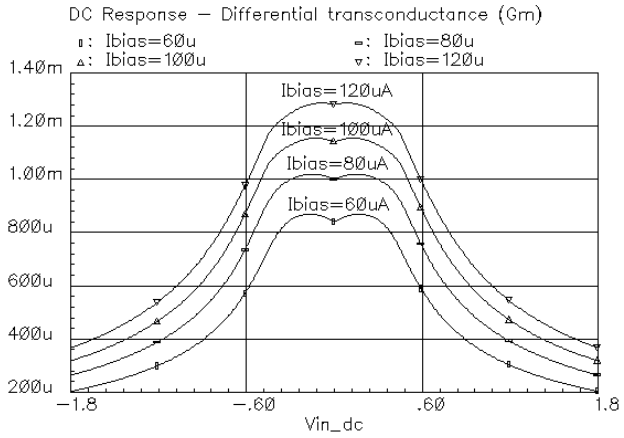

Figure 8. Differential transconductance value of the G_m transconductor for different values of the bias current (**I_{bias} = (60 ÷ 120)µA**)

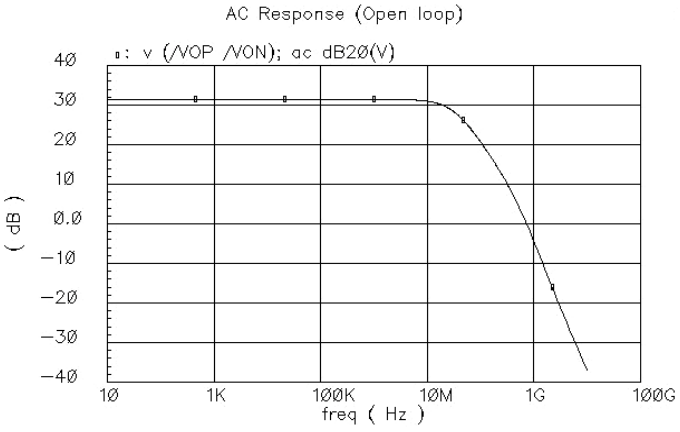

Figure 11. AC frequency response of the G_m in open loop (**I_{bias}=80µA, R_{load} = 1MΩ**)

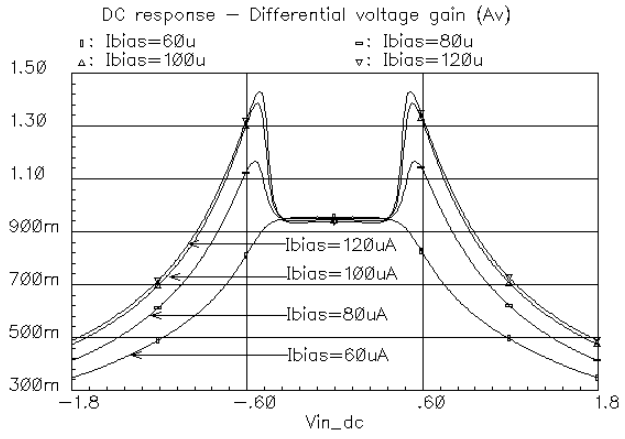

Figure 9. Differential voltage gain of the test circuit from Fig. 5 for different values of the bias current (**I_{bias} = (60 ÷ 120)µA**)

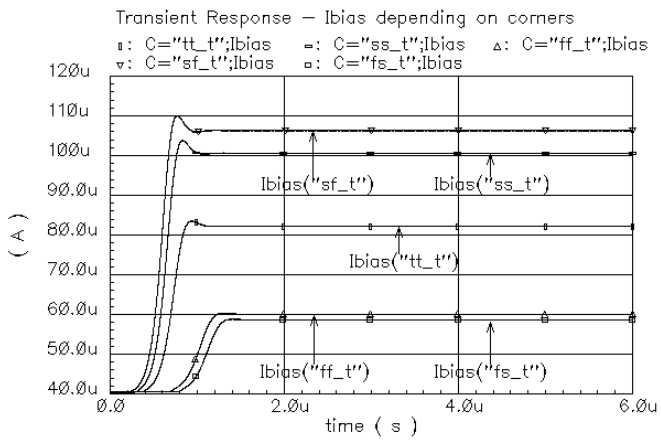

Figure 12. Bias currents I_{bias} depending on the corners:
tt_t: **I_{bias} = 82.2µA**; ss_t: **I_{bias} = 100.6µA**;
ff_t: **I_{bias} = 60µA**; sf_t: **I_{bias} = 106.2µA**;
fs_t: **I_{bias} = 58.6µA**

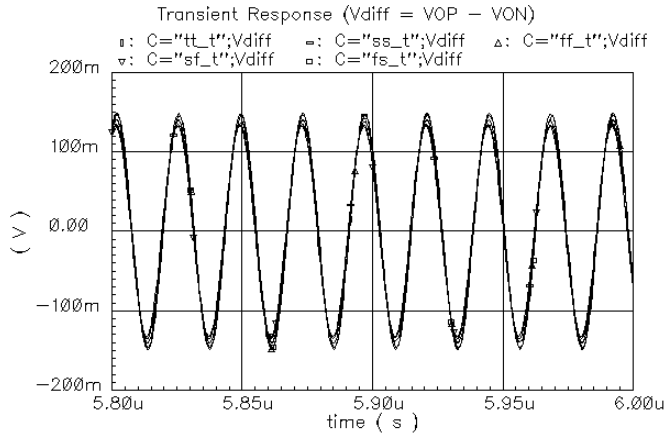

Figure 13. Differential output voltage of the proposed LPF with auto-tuning loop depending on the corners for a 42MHz input signal with $400mV_{pp(diff)}$ magnitude

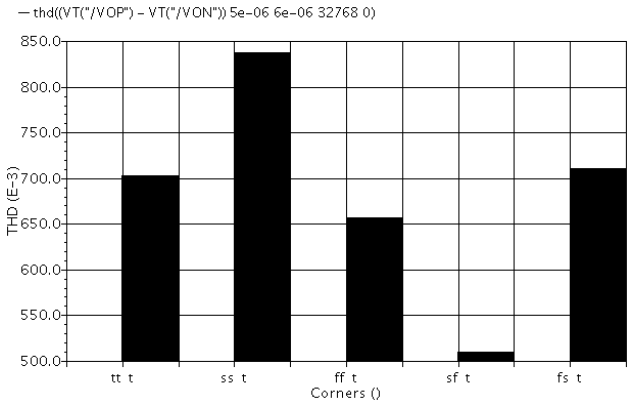

Figure 16. THD of the differential output voltage of the proposed LPF with auto-tuning loop depending on the corners for a 42MHz input signal with $400mV_{pp(diff)}$ magnitude

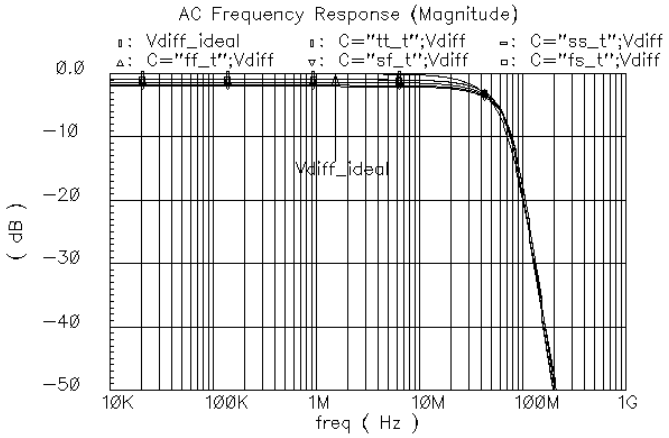

Figure 14. AC frequency response (magnitude) of the proposed LPF with auto-tuning loop depending on the corners
(Bias currents $\boldsymbol{I_{bias}}$ are provided by the auto-tuning loop - Table 3)

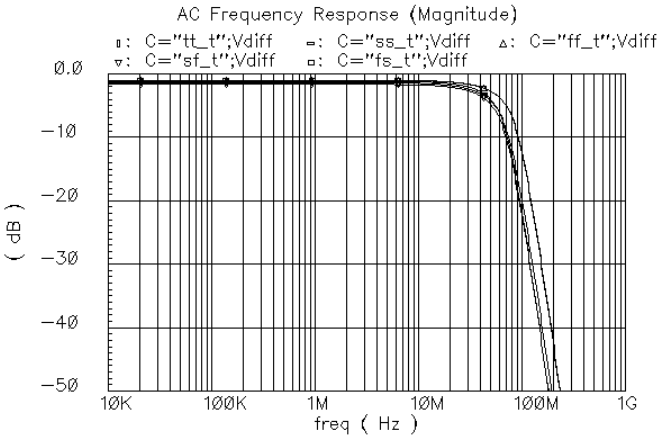

Figure 17. AC frequency response (magnitude) of the proposed LPF with constant bias currents depending on the corners
($\boldsymbol{I_{bias}}$ = 80µA)

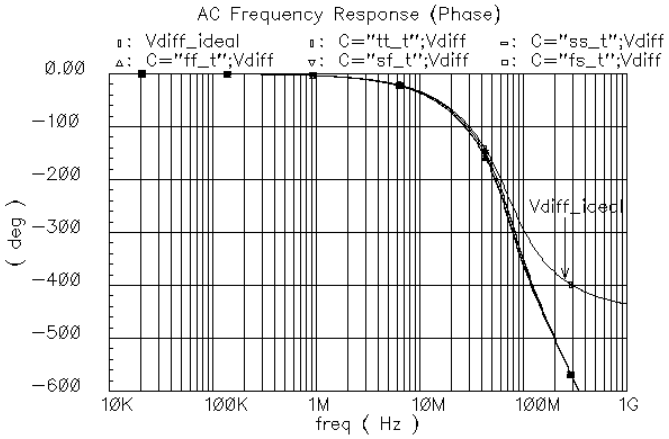

Figure 15. AC frequency response (phase) of the proposed LPF with auto-tuning loop depending on the corners (Bias currents $\boldsymbol{I_{bias}}$ are provided by the auto-tuning loop - Table 3)

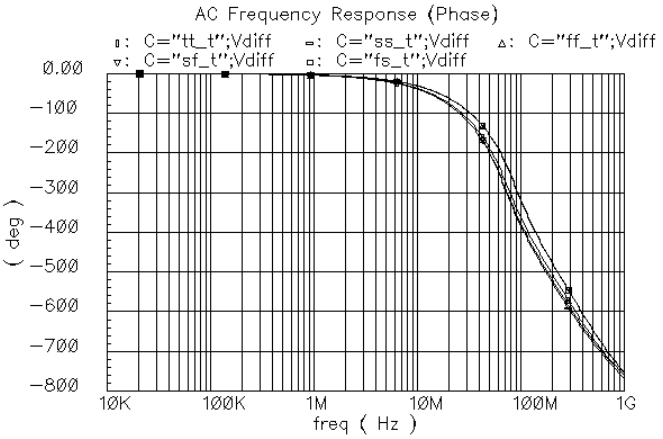

Figure 18. AC frequency response (phase) of the proposed LPF with constant bias currents depending the on corners
($\boldsymbol{I_{bias}}$ = 80µA)

TABLE 3. BIAS CURRENTS PROVIDED BY THE AUTO-TUNING LOOP DEPENDING ON CRITICAL CORNERS

Critical corners (process, temperature, supply voltage)	**Bias current provided by the auto-tuning loop [μA]**
tt_t (typical), 75°, PS=1.8V	82.2
ss_t (slow-slow), 125°, PS=1.62V	100.6
ff_t (fast-fast), 0°, PS=1.98V	60
sf_t (slow-fast), 125°, PS=1.62V	106.2
fs_t (fast-slow), 0°, PS=1.98V	58.6

From these simulations a small corners variation of the common-mode voltage between (870 – 910)mV has been obtained.

Next, by using the corners dependent bias currents from Table 3, the AC simulation of the 5th order differential ***G_m-C*** Bessel type low-pass filter with auto-tuning loop in Fig. 1 is performed, using the grounded capacitor values illustrated in Table 2.

In Figs. 14 and 15 the small signal frequency responses (magnitude and phase versus frequency) of the proposed 5th order differential ***G_m-C*** Bessel type low-pass filter with auto-tuning loop in Fig. 1, for a cut-off frequency of 42MHz are presented by AC simulations performed in all critical corners illustrated in Table 3.

In order to validate the Bessel type characteristics, the Bode characteristics provided by the proposed LPF (shown in Figs. 14 and 15) are compared with the ideal ones given by the ideal 5th order differential ***G_m-C*** Bessel type low-pass filter (shown in Fig. 3), implemented at the system level. From Figs. 14 and 15 we can see that a magnitude and phase responses of the proposed LPF are very close to the ideal ones in Fig. 3.

According to these simulations results, the 5th order differential ***G_m-C*** Bessel type low-pass filter with auto-tuning loop provides a ±5% corners variation of the cut-off frequency.

In Fig. 16 the THD values of the differential output voltage of the proposed 5th order differential ***G_m-C*** Bessel type low-pass filter with auto-tuning loop in Fig. 1, for a 42MHz input signal with $400mV_{pp(diff)}$ magnitude are presented by transient simulations performed in all critical corners. From these simulations a $\boldsymbol{THD \leq 1\%}$ have been obtained for all critical corners and cut-off frequencies imposed by design conditions.

In Figs. 17 and 18 the small signal frequency responses (magnitude and phase versus frequency) of the proposed 5th order differential ***G_m-C*** Bessel type low-pass filter with constant bias currents ($\boldsymbol{I_{bias} = 80\mu A}$), for a cut-off frequencies of 42MHz are presented by AC simulations performed in all critical corners illustrated in Table 3.

According to these simulations results, the 5th order differential ***G_m-C*** Bessel type low-pass filter with constant bias currents provides a ±20% corners variation of the cut-off frequency.

These simulations performed in a 65nm CMOS technology confirm a match better behavior of the proposed 5th order differential ***G_m-C*** Bessel type low-pass filter with auto-tuning loop (±5% corners variation of the cut-off frequency) than the same LPF which uses the constant bias currents (±20% corners variation of the cut-off frequency).

VI. CONCLUSION

In this paper a new low voltage 5th order differential ***G_m-C*** Bessel type low-pass filter with auto-tuning loop and higher dynamic range has been presented.

The proposed architecture provides a cut-off frequency independent of the process, supply voltage and temperature variations. This is done by using an auto-tuning loop, which provides the bias currents used by the LPF core, keeping the ***G_m/C*** ratio independent of these variations.

In order to put in evidence the performances of the designed LPF, the operation of the proposed circuit with auto-tuning loop has been compared with the same circuit, but using constant bias currents. The proposed structure provides a ±5% variation of the cut-off frequency in all critical corners, a $400mV_{pp(diff)}$ dynamic range, THD<1% and 21.6mW power consumption from 1.8V supply voltage.

The simulations have been performed in 65nm CMOS process and confirm the theoretical results.

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