Cyber Physical Systems: A New Approach to Power Electronics Simulation, Control and Testing

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***Abstract*—This paper presents a Cyber Physical Systems approach to power electronics simulation, control and testing. We present a new framework based on generalized hybrid automaton and application specific ultra-low latency high-speed processor architecture that enables high fidelity real-time power electronics model computation. To illustrate the performance of this approach we experimentally demonstrate two extremely computationally demanding power electronics applications: real-time emulation for Hardware-in-the-Loop (HIL) testing, and hybrid system observers for fault detection and isolation.**

***Index Terms*—power electronics, real-time systems, hybrid intelligent systems, computational modeling, observers.**

I. INTRODUCTION

Cyber physical systems (CPS) represent tight integration and coordination of computation and physical processes [1]. Potential applications of CPS range from process control, advanced automotive control systems, traffic control, and robotics all the way to power electronics and smart grid, to name a few. The intimate coupling between computational layer and physical layers has a potential to bring significant benefits in terms of overall system performance, functionality, reliability, and fault-tolerance. Arguably, the application of CPS to energy conversion and in particular to control and coordination of smart grids and power electronics, as one of smart grid's key physical layers, is one of the key CPS applications, as it is poised to bring innumerable benefits to our society in terms of energy efficiency, sustainability, and overall environmental impact[2], [3].

CPS is not a completely new concept. Embedded systems are considered as its predecessor since in embedded systems digital processors monitor and control physical processes, most often in a feedback loop configuration, in such a way that the computation affects physical layer and vice versa. While embedded systems have been widely successful, CPS present the next revolutionary step in the development towards high-performance, highly networked, ultra reliable embedded systems.

In order to achieve the full potential of CPS approach fundamental rethinking of real-time modeling, computation, networking, simulation, testing, and control is needed [1]. The key motivation for revisiting and re-inventing some of the prevailing computational paradigms stem from the fact that physical processes are intrinsically time driven and concurrent while most of the computational and software platforms were developed and optimized for data centric systems and hence lack proper abstractions and specific implementations to deal with hard real-time requirements. Indeed, this limitation manifests trough the lack of time predictability both in terms of computation and communication capabilities.

In this paper we focus on the application of CPS to power electronics modeling, simulation, control, and testing. We adopt the hybrid system modeling approach to power electronics which naturally lends itself to efficient and time predictable computation. Furthermore, we present a new processor architecture that is tailored for ultra-fast real-time computation - featuring time predictable execution. To demonstrate the new capabilities of proposed CPS approach, based on hybrid system modeling and new digital processor architecture, we examine two critical high performance power electronics applications: real-time emulation for Hardware-in-the-Loop (HIL) [4], and hybrid system observers for fault detection and isolation [5].

The paper is organized in five sections. Section II gives a brief overview of the hybrid system modeling framework and how it pertains to power electronics. Section III presents an application specific processor architecture that is tailored for real-time emulation of hybrid systems with ultra-low latency and high-speed. Two illustrative examples, together with experimental results, are given in Section IV. Finally, Section V summarizes the paper and outlines potential new applications for the ultra-low latency processor.

II. HYBRID DYNAMICAL SYSTEM MODELING

Power electronics (PE) systems are inherently non-linear, switched circuits where the control of power flow is achieved with precisely timed switching events [6]. Generic block diagram of PE converter is shown in Fig. 1.a). The combination of continuous time dynamics (continuous-time state-space) and discrete events (finite automaton) that PE exhibits lends itself naturally to hybrid system modeling approach. This motivated us to adopt the modeling framework based on Generalized Hybrid Automaton (GHA) with the piecewise linear continuous dynamics [7].

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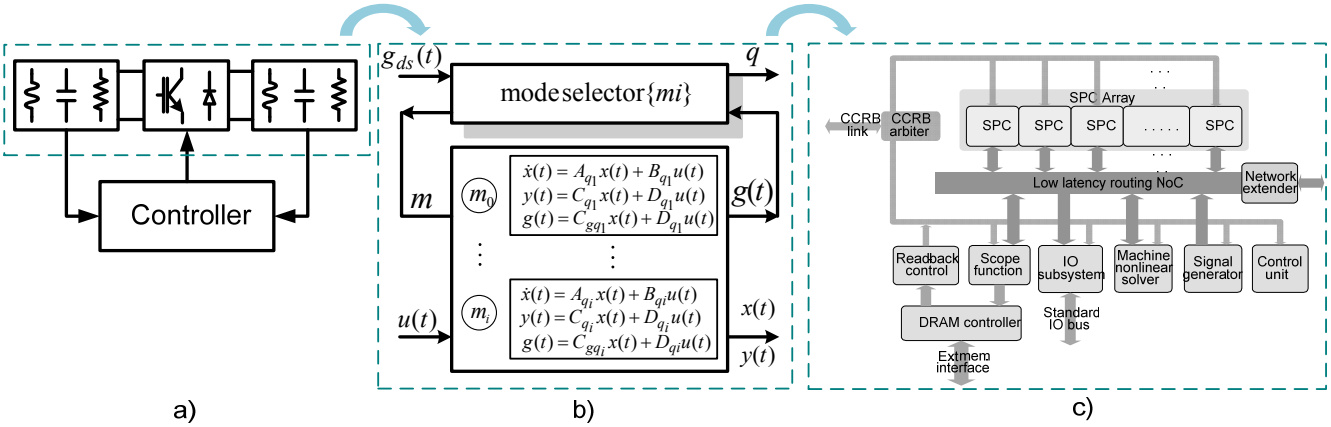

Figure 1. Diagram of power electronics model abstractions, from circuit, to GHA towards digital implementation. a) Circuit abstraction, b) Hybrid automation abstraction of power electronics system, c) Digital implementation on application specific multi-core processor architecture where models and finally ported are finally ported and executed in real-time.

Power electronics circuit elements are represented with: passive elements (R, L, and C), piece-wise linear switches, current and voltage sources (both controlled and independent) that yield a piecewise linear state space representation, shown in Fig. 1.b), that can be represented as:

$$\dot{x}(t) = A_{q_i}\dot{x}(t) + B_{q_i}u(t) \quad (1)$$

$$y(t) = C_{q_i}x(t) + D_{q_i}u(t) \quad (2)$$

where $x(t) \in R^n$ is continuous state space vector, $y(t) \in R^k$ is the output vector, $u(t) \in R^m$ is the input vector; $A_{q_i} \in R^{nxn}$ and $B_{q_i} \in R^{mxm}$ are state space matrices. Any discrete state of the circuit belongs to a finite set $Q = \{q_1 \cdots q_m\}$ that further defines given state space representation. Every discrete state q_i therefore has a unique dynamic behavior, that we call a mode. A mode, denoted as m_{q_i}, where $q_i \in Q$, is the operation of the system given by the state space representation given in Eq. (1) and (2) and for a given q_i. Since not all the possible discrete state-to-state transitions are possible, we define a set $E \subseteq Q\,x\,Q$ that uniquely defines the collection of allowable discrete transitions. In addition, each discrete transition $e = (q_i, q_k) \in E$ has assigned switching condition g - guard, that uniquely defines the active mode [7], [8].

III. Hybrid System Tailored Computational Platforms

A. Architecture overview

In order to take the full advantage of the adopted modeling approach we developed a computational platform that can compute GHA models in real-time, with predictable timing, and with good fidelity. The hard real-time requirements imposed on the computational platform translate into the need for ultra-high speed, deterministic, and time predictable:

- model computation
- memory management and
- input/output communication latency.

In order to satisfy all of the above requirements, which none of the off-the-shelf processors can meet, we developed a new architecture, illustrated in Fig. 1.c), and explained in details in [9]. The new digital processor comprises an array of standard processing cells (SPC) which can be thought of as GHA application specific processor cores. Each SPC is fully programmable and solves a GHA sub-model up to a parameterized level of complexity in terms of number of switches and a number of energy storage elements. All SPC units operate synchronously and in parallel, each accessing its individual memory resources only. All units in the time critical data path, with the exception of statically mapped inter SPC communication lines, are connected using the low latency network on chip (NoC); a reconfigurable fabric optimized design. Inter chip (FPGA) connection is provided by high speed serial network extender unit, as shown in Fig. 1.c). The communication that is not latency critical, such as communication with the external PC, is implemented with a dedicated control, configuration and read back bus (CCRB).

To make the architecture as general as possible while providing low latency interface to the test environment, the I/O boards are interfaced on a custom bus level [10]. With this approach I/O board details are hidden from a processing architecture by an I/O board specific glue logic device thus allowing I/O subsystem abstraction.

B. Processor scaling

An industrially applicable solution must scale in order to be applicable to power electronics systems ranging from a simple buck converter to multi-level, multi-drive systems with complex interconnection network.

The proposed design supports three hierarchical levels of scaling:

- inter processor level – a number of processors working on the same problem
- inter SPC level – parameterizable number of SPCs per processor
- intra SPC level – parameterizable number of execution units per SPC elements

C. Standard processing cell (SPC) design

Each SPC unit comprises two functional units: a programmable topology selector and a linear state space equation solver. To meet performance and programmability requirements the programmable topology selector implementation borrows heavily from the field of

telecommunications [11]-[13]. Building on the results from [14], the proposed solution further customizes the basic processor design by means of:

- VLIW (very large instruction word) architecture with parameterizable number of customized execution units,
- complete absence of Arithmetic Logic Unit (ALU) since all the arithmetic tasks are mapped to linear solver,
- introduction of execution start address look aside table for instant program counter (PC) positioning based on current state and input values,
- register file reduced to a state register only.

The result of the proposed improvements is an area efficient design capable of extremely short state decision time, which is, for a typical three-phase converter on the order of 10 clock cycles.

D. Linear solver

The PE modeling is based on the state space representation with exact fixed time step discretization required for deterministic time execution on real-time system platform.

The piece-wise linear part of each sub-system is represented with a complete set of state-space representations mapping all reachable sub-model topologies. The matrices are computed off-line, as a part of the model compilation process, and stored within the dedicated matrix memories. The topology switching, controlled by topology selector [15], [16], is implemented using direct memory indexing technique. Since all state space representations are time-invariant (over a simulation time step) there is no need to recalculate the matrices during the runtime and the task of linear solver is to compute system state space vector based on the discretized model.

$$\begin{bmatrix} x((k+1)T) \\ y(kT) \end{bmatrix} = \begin{bmatrix} A_d(T) & B_d(T) \\ C_d & D_d \end{bmatrix} \cdot \begin{bmatrix} x(kT) \\ u(kT) \end{bmatrix} \tag{3}$$

where x is the state space vector, u is the input vector, A_d, B_d, C_d, and D_d are system matrices, and T is the simulation time step. We use the exact discretization method via state-transition matrix where discretized system matrices are given as:

$$\begin{aligned} A_d(T) &= e^{AT} \\ B_d(T) &= \int_{kT}^{(k+1)T} e^{A[(k+1)T-\tau]} \cdot B \cdot d\tau \end{aligned} \tag{4}$$

under the assumption that $u(t)$ is piecewise constant during the simulation time step. Therefore (4) becomes:

$$\begin{aligned} A_d(T) &= e^{AT} \\ B_d(T) &= [e^{AT} - 1] \cdot A^{-1} \cdot B \end{aligned} \tag{5}$$

which is calculated off-line and stored in the dedicated processor memory.

IV. Application Examples

The proposed approach to CPS applied to power electronics, that combines the GHA modeling and ultra-low latency high-speed processor architecture, enables hard real time computation with 1 μs time step and latency of complex hybrid systems. Now, we will examine two applications that are enabled by this approach, namely ultra-high fidelity real-time emulation of power electronics circuits for hardware-in-the-loop simulation and hybrid model-based observers for fault detection and isolation.

A. Hardware in the Loop (HIL)

Real-time digital emulation (simulation) makes it possible to replace a physical system with a computer model for the real-time control design, testing, and optimization. This concept is illustrated in Fig. 2, where a detailed model of an induction motor electric vehicle drive with two-level inverter is emulated on the HIL emulation platform from [9]. HIL emulator interacts with the real physical controller, in this case TI ezDSP F2812 based controller platform, via fast input/output signals in real-time. This controller takes some signal for HIL platform and based on them and control algorithm generates appropriate control signals.

From the controller perspective there is no difference between the physical system and its real-time simulation. Indeed, the real controller (and here we mean also the high speed part of the controller which includes the modulator and the protection functions) "feels" that it is controlling the real physical system.

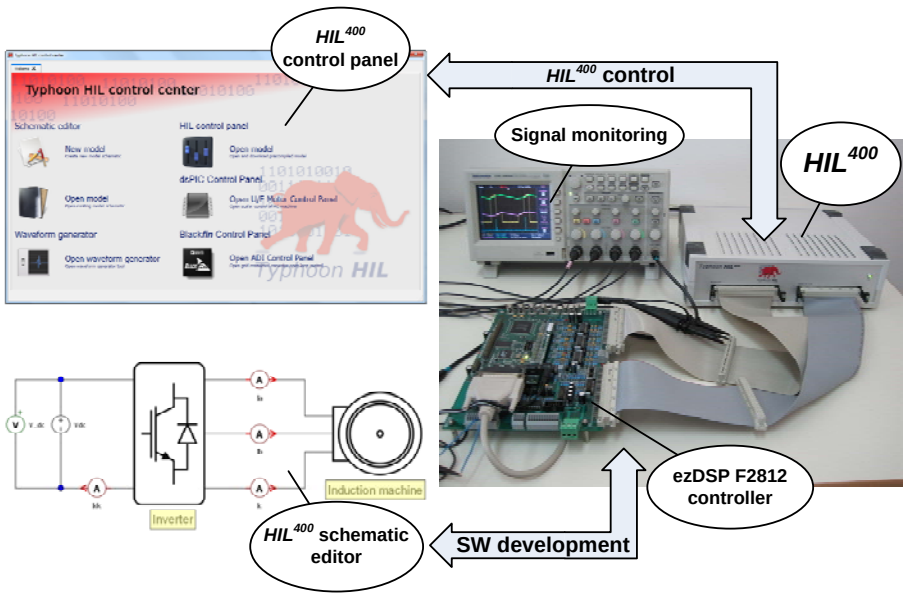

Figure 2. Complete HIL development environment comprising TI DSP F2812, Real-time HIL emulator, and integratd software environment for both HIL control and DSP code development and debugging.

Real-time digital emulation as a means of testing control systems is not a new idea. For example, the automotive industry has been using it since software became a safety-critical component of the automotive electric/electronic systems [17]. Indeed, there are four compelling reasons for using real-time HIL emulation in power electronics that can be summarized as:

- reduction of development cycle,
- demand to extensively test control hardware and software in order to meet performance, safety and quality requirements,
- the need to prevent costly failures, and
- increased availability of hardware in the loop [18]

Power electronics applications comprise a number of controlled switches that are highly demand to simulate accurately in real time. [19] Power electronics circuits are also highly non-linear and need very tiny time steps to reach acceptable level of accuracy. With the conventional off-the-shelf computers, it is very difficult to achieve small simulation time steps. Due to extremely low latency requirements and regarding for accurate simulation only FPGA technology can provide ultra low latency [20], [21].

To illustrate all above points consider a variable speed e-car drive, shown in Fig. 3, where power flow and motor speed and torque are controlled with a two-level IGBT inverter operating at a switching frequency of several kHz. Our platform, can emulate this system in real-time with high-fidelity and simulation time step of 1μs which accounts for both latency and computation time. This is almost two orders of magnitude improvement compared to today's state of the art, 50 μs time-step, commercially available digital HIL systems.

1) HIL Fidelity Testing

In order to test the fidelity of proposed emulator platform based on hybrid automaton PE modeling and ultra-low latency high-fidelity digital processor we designed a series of tests where both real PE converter and equivalent HIL system are controlled with the same controller, as shown in Fig. 3.a). Measured waveforms on both the real system and the emulator are shown in Fig. 3.b), with almost one-to-one matching. Emulator response latency is measured to be less than(1.3 μs), as shown in Fig. 3.c)

2) Fault Injection Emulation with HIL

Another important benefit of HIL testing approach is the ability to easily inject both soft and hard faults—which are difficult or sometimes even impossible to do in a safe and controllable way with real PE hardware—during the converter operation. Soft faults are the ones where the structure of the circuit is preserved, i.e. change in the value of passive elements (R, L, C). Hard faults are the ones where the topology of the circuit is changed upon fault injection, i.e. short-circuit or open-circuit fault. Both of these fault modes are extremely important to test the control system robustness and design graceful fault-mitigation strategies.

To demonstrate the hard-fault injection capability we show the open-phase fault injection and corresponding real-time signals in Figure 4 and Figure 5.

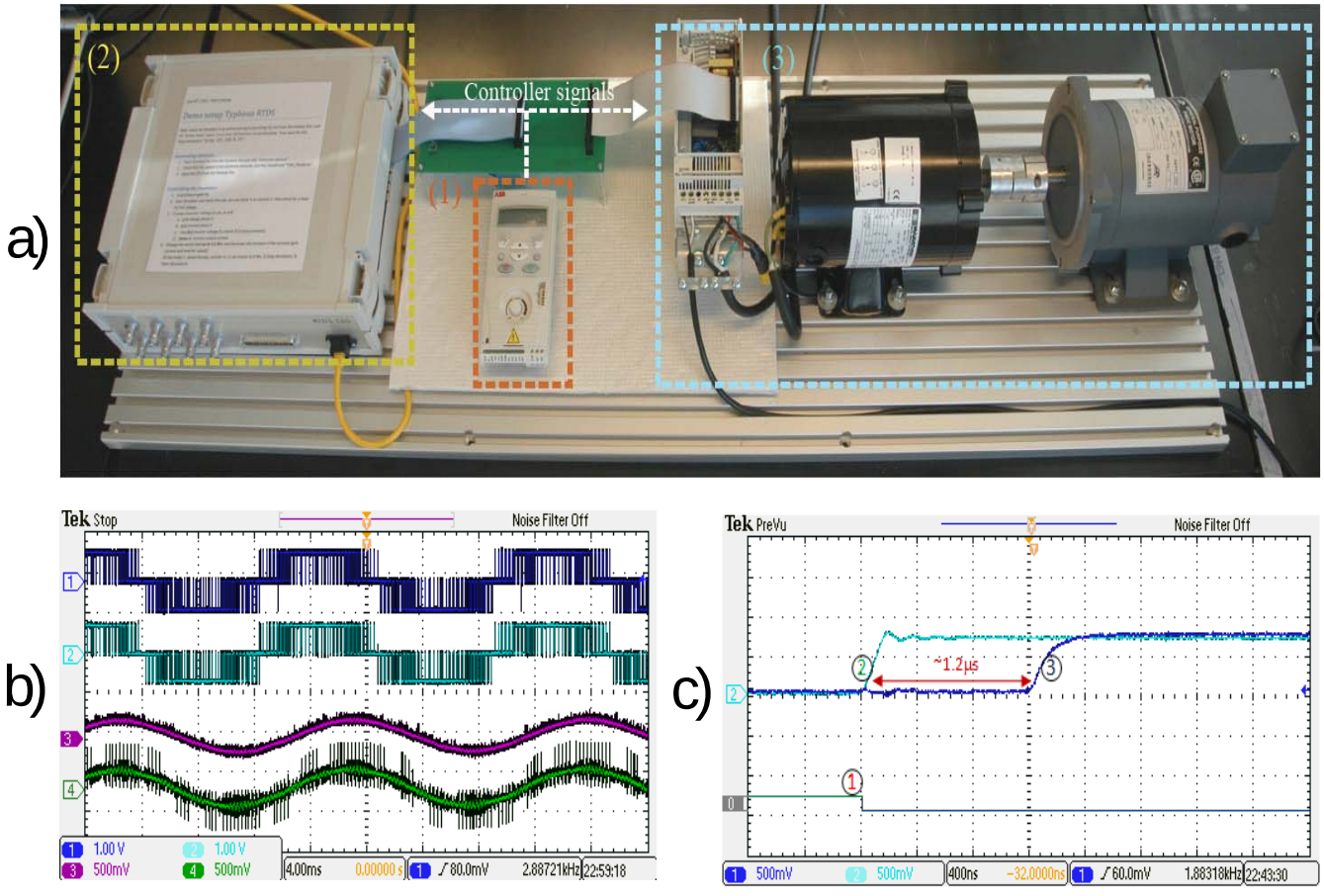

Figure 3. a) HIL fidelity test setup with the controller simultaneously controlling both the real 2-level inverter-induction motor-load system, and HIL emulator b) comparison of real hardware and HIL inverter line-to-line voltages and phase currents. c) latency compariosn from gate drive to line-to-line inverter voltage.

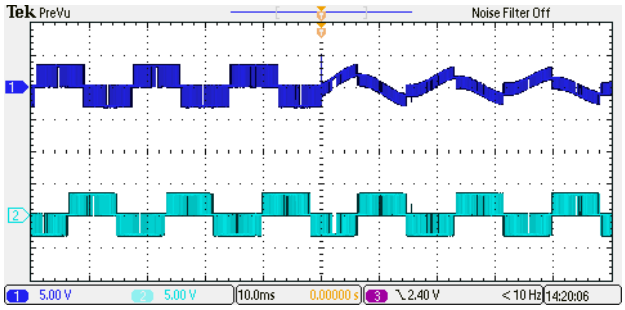

Figure 4. Open phase fault at $t = 0\,s$. HIL emulation response is observed for the line-to-line voltages (V_{ab} and V_{ac} , 100 V per div)

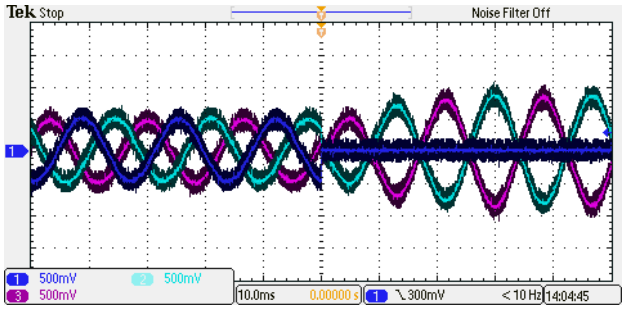

Figure 5. One phase fault at $t = 0\,s$. HIL emulation response is observed for the line-to-line voltages (V_{ab} and V_{ac} , 100 V per div)

B. Fault detection and Isolation

Model based fault detection, based on the piecewise linear observers is another important application that is becoming practical thanks to generalized hybrid automaton power electronics modeling approach and proposed ultra-low latency high-fidelity digital real-time processor platform [22], [23].

Although averaged and linearized models of PE were used in the past to design observers, and in particular fault detection and isolation observers, due to inherent nonlinearity of PE circuits these observers were not able to capture and reproduce high-speed transients and dynamics that is on the order of the switching frequency of the converter, hence seriously impeding its dynamical performance and its fault detection [5].

The typical structure of the hybrid observer is given in Figure 6, following approach proposed in [5] and [24]:

$$\dot{\hat{x}}(t) = A_{q_i}\hat{x}(t) + B_{q_i}u(t) + L(y - \hat{y}) \tag{6}$$

$$\hat{y}(t) = C_{q_i}\hat{x}(t) \tag{7}$$

Fig. 7 demonstrates the observer fault signature (red trace) upon open phase fault injection. (when one phase is opened) Before the fault occurs, fault signature is zero, while it immediately jumps to a large non-zero value once the fault was injected in the observed system. Similarly, on the same figure we can see the degradation of DC-link capacitance and how it reflects on fault signature signal (red trace).

This concept enables almost instantaneous (within one time step, 1μs fault detection and isolation unlike previous observers that were based on linearized average PE models. Furthermore, this approach can be extended to reduced model observers, Model Reference Adaptive Controllers, Kalman observers providing a whole new level of dynamic performance and fidelity.

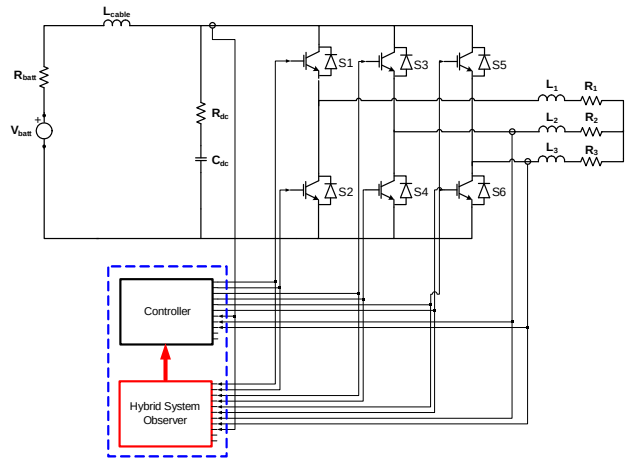

Figure 6. Schematic block diagram of 2-level inverter with controller and piecewise linear model-based fault detection observer

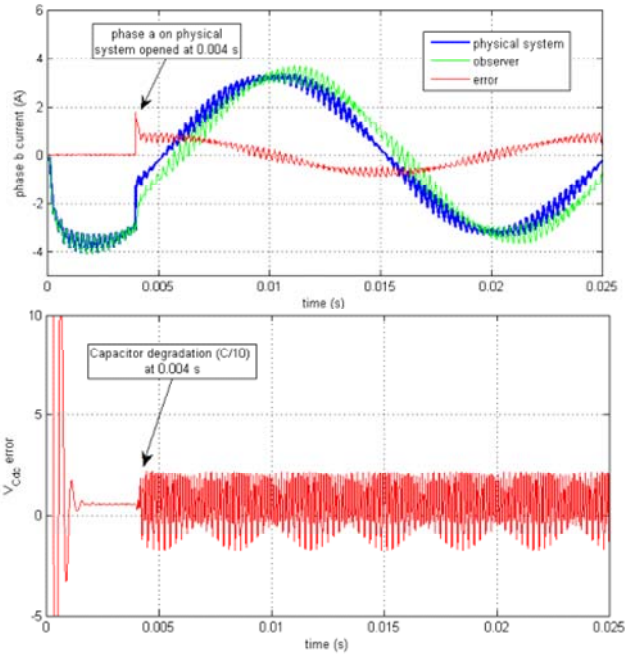

Figure 7. Fault detection signal (red) upon phase open fault. and fault detection signal upon DC-link capacitor degradation

V. Conclusion and Future Research Direction

In this paper we have demonstrated the application of one aspect of cyber physical systems approach to power electronics modeling, simulation, control, and testing. We presented the generalized hybrid system modeling approach to power electronics which is naturally suited for high-efficiency and time predictable computation. Furthermore, we demonstrated that GHA application specific processor architecture enables computation with 1μs time step of complex power electronics models. Furthermore, we experimentally demonstrated real-time computation for: Hardware-in-the-Loop emulation, and hybrid system observer for fault detection and isolation with dynamic performance unachievable with any other approach both in terms of dynamic performance and fidelity.

We believe that proposed CPS platform will find use in other high-performance control and computation applications ranging from hybrid controllers, estimators, all the way to real-time finite difference and finite element electromagnetic solvers and further.

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