A Performance Analytical Strategy for Network-on-Chip Router with Input Buffer Architecture

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[1]***Abstract*—In this paper, a performance analytical strategy is proposed for Network-on-Chip router with input buffer architecture. First, an analytical model is developed based on semi-Markov process. For the non-work-conserving router with small buffer size, the model can be used to analyze the schedule delay and the average service time for each buffer when given the related parameters. Then, the packet average delay in router is calculated by using the model. Finally, we validate the effectiveness of our strategy by simulation. By comparing our analytical results to simulation results, we show that our strategy successfully captures the Network-on-Chip router performance and it performs better than the state-of-art technology. Therefore, our strategy can be used as an efficiency performance analytical tool for Network-on-Chip design.**

***Index Terms*—Network-on-Chip, Semi Markov process; Modeling, Queuing theory, Simulation**

I. INTRODUCTION

With the development of deep sub micrometer (DSM) technologies, more and more processors can be integrated on a single chip. When there are hundreds, even thousands homogeneous or heterogeneous IP (Intellectual Property) cores, the traditional Bus architecture can not satisfy the inter-communication requirement gradually. In order to solve this problem, the concept of NoC (Network-on-Chip) [1][2] was proposed.

The main difference between NoC and the computer network is the restrictions in the amount of resources and the power consumption [3]. Generally speaking, NoC requires low network delay, high throughput, low power consumption and small chip area [4]. Besides, the time-to-market for customized NoC places a tremendous pressure on the design team [5]. If we evaluate the NoC performance through the time-consuming simulation in NoC design, the development of NoC will be restricted. In order to complete the NoC design fleetly, P.Lieverse in [6] propose a method for NoC design, which depends critically on the availability of adequate performance analysis tools that can guide the overall design process. Time consuming simulations can only be used at later stages, typically after the design space is already reduced to only a few practical choices. In this situation, an efficient performance analytical tool is meaningful for NoC's development. Because the NoC is proposed to solve the bottleneck of on chip communication, the average packet delay in NoC is one of the most important guidelines in NoC performance evaluation [7]. Moreover, since routers are the infrastructure of NoC, it is important to develop a method to analyze the router performance if we want to get the average packet delay in NoC [8].

Based on the mentions above, this paper proposed a performance analytical strategy for NoC router. First, a SMP (Semi-Markov Process) [9] is proposed to describe the mechanism of NoC schedule. By using the SMP model, both the average schedule delay and the average service time can be calculated. Second, we calculate the average packet sojourn time in router and the queuing characters of buffers to analyze the router performance. Finally, we validate the effectiveness of our model by simulation and compare it with the state-of-art technology.

The paper is organized as follow: in the second section, we give the related work briefly. The router architecture and the model assumptions are given in the third section. In the fourth section, we define some related parameters, develop a model and analyze the router performance. In the fifth section, we validate the effectiveness of our strategy by simulation. Finally, we summarize our contribution.

II. RELATED WORKS

Because the restriction of the resources, complex flow control protocol may not be suitable for NoC [10]. At present, backpressure mechanism, which makes the data can't be transmit to downstream router when the related downstream buffer is full, is often used in NoC [11][12]. Under this mechanism, NoC router works as a non-work-conserving infrastructure and it is different with the work conserving router in other network domain. On the other hand, buffer size in NoC is finite, which is different with some network domains, too. Therefore, although there are a lot of analytical model for network and router, they can't be directly used for the NoC domain [13].

In computer network and some network related domains:

Dimitrios in [14] proposed a LR (Latency Rate) model to analyze the maximal end to end delay for some schedule algorithm. However, the model is built for the work conserving network, it isn't suitable for NoC router.

Fabio M in [15] proposed a RST (Rate Spaced Timestamp) model for GPS (Generalized Processor Sharing) related schedule algorithms to analyze the end to end delay in the worst case. However, the model is based on work conserving mechanism and it thus can't be used for NoC router directly.

V.S.Adve in [16] proposed a method to analyze the network performance with determinate routing algorithm. However, the router buffer size in the model is assumed to be one flit, which can't be used directly for NoC when the

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router buffer sizes are changed.

Le Boundec in [17] proposed a network calculus method, which can be used to compute the minimal buffer size. However, when the buffer size is small, the bound drive in [17] can be loose and the model can not get the NoC performance precisely.

In NoC domain, there are two kinds of methods to evaluate the NoC router performance, one method is to get the performance by simulation, which is time consumption but can get the result precisely, and another method is to get the performance through analytical models, which can analyze the NoC router performance rapidly.

Chang Wu in [18] and Narasimhan A in [19] propose their NoC router design method and evaluate the router performance. However, they get the router performance by simulation, which need a lot of time.

Paul Beekhuizen in [20] proposed an analytical model for a tandem NoC and computed the average packet sojourn time for router with different scale of crossbar. However, the model hasn't taken the block probability of downstream router into consideration, which make the model unsuitable for the router in NoC with other topologies.

Guz.Z in [21] proposed a method to analyze the performance of QNoC and optimize the link capability. However, the model is suitable for asynchronous NoC, in which router need both input buffer and output buffer. Therefore, the router architecture in [21] is different with the classical router architecture.

S. Murali in [22] evaluate the average packet delay in NoC by the number of hops, it is usable for NoC router under GT (Guarantee Through) mode. However, for the NoC router under BE (Best Effort) mode, the method in [22] can not capture the performance of router.

Jingcao Hu in [23] proposed a system level analytical model for NoC to solve the BAP (buffer allocation problem). However, the model in [23] assumed that there was no conflict among buffers in the same router. Although it may not be a serious problem for BAP, we can't get the router performance precisely through the model.

We in [24] proposed a model for NoC with finite buffer size for buffer size optimizing. However, the model in [24] dose not consider the conflict among buffers in the same router, too. Therefore, the model can not capture the router performance precisely.

III. Router Architecture and Model Assumptions

In [24], we have discussed that how to develop the analytical model of a single router to the whole NoC. Therefore, in this paper, we only build an analytical model for a signal router as shown in Fig.1. Fig.1 shows the classic NoC router architecture with input buffers, where AD is used to detect the destination address for packets, CS is used to generate requirement for the next hop, Crossbar is used to transfer the packets to the downstream router, Arbiter is the module to realize the schedule and routing algorithm, and FIFO is used to storage the packets as first come first out mode.

The model is developed with the follow assumptions:

1. The buffer size is finite and small, and the packets are transmitted based on virtual cut through mechanism. When several FIFO require the same output port, one FIFO can be authorized by schedule algorithm (in this paper, we use the Lottery algorithm).
2. Backpressure mechanism is adopted to control the packet transfer. When the required downstream buffer is full, packets have to be stored in the local buffer.
3. In the input ports of a router, the input packet are independent with each other and the packet arrival process obeys the Poisson distribution. The packets can't require the output port in the direction where the packets come from.
4. The number of flit is used to describe the packet size. In one clock period, only one flit can be transmitted to the downstream buffer.
5. Only one clock is used in the router.

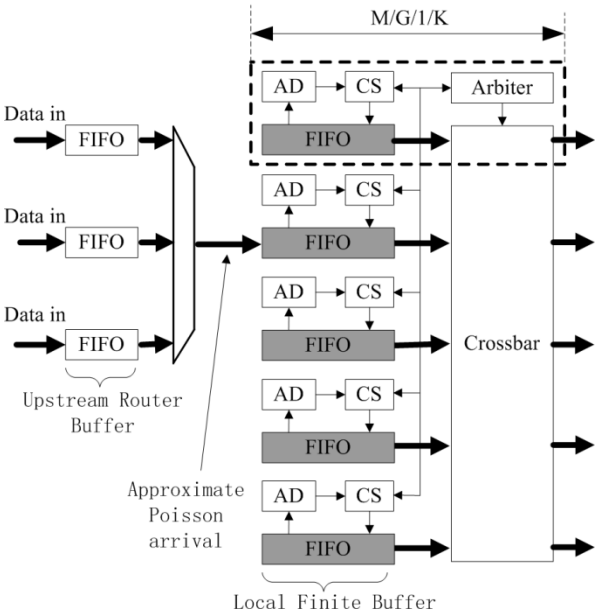


Figure.1 The classic router architecture in NoC

IV. Analyzing and Modeling

In order to develop the model conveniently, we define some parameters as table 1. After we define the parameters, we develop our model.

In order to get an accurate model for evaluating the router performance, a Semi-Markov process is proposed to describe the behavior of the FIFO head. First of all, the behavior of a channel is partitioned into four disjoint work states.

State 0 is the preprocessing subset that the FIFO head is waiting the coming packet and generating the requirement signal.

State 1 is the processing subset that the router is processing the packet which has been authorized to access the downstream buffer (in state 1, the packet will be transmitted to the downstream FIFO. However, if the downstream FIFO is full, the packet may be blocked until the downstream FIFO is not full).

State 2 is the full waiting subset. The process enters state 2 when several buffers attempt to access the same output port simultaneously and one of other required buffers is selected to access the downstream buffer. In state 2, the buffer has to wait until the packet in the selected buffer was processed.

State 3 is the residual waiting subset. The process enters state 3 when the packet in the buffer head requested a

downstream buffer and it found that the downstream buffer was being accessed by another buffer of this router.

TABLE 1 PARAMETERS

η_i	The average time that the head of FIFO sojourn in the state *i* of SMP
P_b	The block probability of the related downstream buffer
M	The packet length
C	The average interval between two tandem packets in the FIFO head
S_{next}	The average service time of the downstream buffer
a_{ij}	The probability that the state in SMP conversion from state *i* to state *j*.
WIN	The probability that FIFO is authorized by the schedule algorithm when it compete the output port with other FIFO
BUSY	The probability that a FIFO finds the related downstream FIFO is accepting packet from other FIFO
π_i	The steady probability of state *i* in Markov chain
P_i	The limiting probability of state *i* in SMP
R	The probability that FIFO request to access a particular downstream FIFO
l_i	The rate of leaving state i
D	The average schedule delay
S	The average service time for the local FIFO, which is from the time that requirement is generated to the time that the tail of packet is transmitted.
ρ	The utilization rate of FIFO
λ	he average packet insert rate of FIFO
K	The number of packets that the FIFO can storage
k_m	The probability that there are *m* packets arrived during the time that one packet is processed
π_i^{∞}	The steady probability that there are *i* packets in M/G/1 queuing system
π_i^{K}	The steady probability that there are *i* packets in M/G/1/K queuing system
H	The average sojourn time of packet in local FIFO

Based on the mechanism of NoC, the state transition diagram can be sketched as Fig.2:

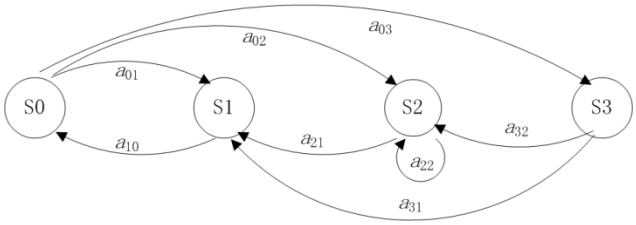


Figure.2 the state transition diagram of FIFO head

Because the transition probabilities in Fig.2 are not related with the states in previous time and only related with the state in the current time, and the sojourn time in each states is not a constant value, the progress of FIFO head is a SMP, and the embedded Markov chain is irreducible with ergodic states. Therefore, P_i (the limiting probability of state *i*) and l_i (the rate of leaving state *i*) can be express as:

$$P_i = \frac{\pi_i \eta_i}{\sum_{j=0}^{3} \pi_j \eta_j} \tag{1}$$

$$l_i = \frac{\pi_i}{\sum_{j=0}^{3} \pi_j \eta_j} \tag{2}$$

From the state transition diagram, we can find that the average schedule delay D is the average time from leaving state 0 to coming into state 1 for the first time (Note that once the process comes into state 1, the packet in the FIFO head has been authorized and it can be transmitted to the downstream FIFO), and the average service time S for a local FIFO is the average time from leaving state 0 to return to state 0 for the first time. In order to calculate S and D, the sojourn time η_i in each state can be expressed as (3):

$$\eta_i = \begin{cases} C & i = 0 \\ (1-P_b)M + P_b(M + S_{next}) & i = 1 \\ M & i = 2 \\ \dfrac{M}{2} & i = 3 \end{cases} \tag{3}$$

In order to estimate the schedule delay sufficiently, we suppose the FIFO is saturated in this paper. It means that once the packet in FIFO head is processed, another packet will arrive at FIFO head at once. In this situation, C is the time that consumed by the AD and Channel module and can be predetermined. Therefore, η_0 can be calculated.

In order to calculate η_1 , P_{b} and S_{next} need to be predetermined. Since the method to compute P_{b} and S_{next} has been discussed by us in [24], in this paper, we assume that the two parameters are known.

Since only one flit can be transmitted to the downstream buffer and a packet contains M flits, the time that a router transfers an authorized packet can be expressed by M. Therefore, the value of η_2 can by calculated.

If request signals for the busy downstream FIFO are equally likely to occur at any point in time, the average sojourn time in state 3 can be calculated by M/2. At this point, all value of η_i can be calculated.

Now, we calculate the value of a_{ij} (a_{ij} denote the probability that the state in SMP conversion from state *i* to state *j*) and π_i (the steady probability of state *i* in Markov chain).

From Fig.2, we can get the state transition matrix:

$$A = \begin{pmatrix} 0, & a_{01}, a_{02}, a_{03} \\ a_{10}, 0, & 0, \quad 0 \\ 0, & a_{21}, a_{22}, 0 \\ 0, & a_{31}, a_{32}, 0 \end{pmatrix} \tag{4}$$

Based on the NoC mechanism, the state transition can be expressed as:

$$\begin{cases} a_{01} = (1-BUSY)WIN \\ a_{02} = (1-BUSY)(1-WIN) \\ a_{03} = BUSY \\ a_{10} = 1 \\ a_{21} = a_{31} = WIN \\ a_{22} = a_{32} = (1-WIN) \end{cases} \tag{5}$$

Since the FIFO in direction *i* can't require the output port in direction *i*, for the N*N crossbar, there are (N-1) FIFO requiring the same output ports at most. Thus the *WIN* and *BUSY* can be expressed as [25]:

$$WIN = \frac{[1-(1-R)^{N-1}]}{(N-1)R} \tag{6}$$

$$BUSY = \frac{(N-2)}{(N-1)} \times P_1 \tag{7}$$

Based on the NoC mechanism, when packets leave state 0 or state 2 or state 3, FIFO will generate a requirement signal. Therefore, the probability R is:

$$R = \frac{(l_0 + l_2 + l_3)}{(N-1)} \tag{8}$$

Combine the formula from (4) to (8), and take use of $\Pi = \Pi A$ and $\sum \pi_i = 1$, we can get the steady probability for state i in Markov chain π_i and the state transition probability a_{ij}. Then, we can compute the D and S through (9) and (10):

$$\begin{aligned} D &= \sum_{\forall j}\sum_{\forall i} P(T = (i\eta_2 + j\eta_3)) \times T \\ &= P(T=0)\times 0 + \sum_{i=1}^{\infty} P(T = i\eta_2)(i\eta_2) + \sum_{i=0}^{\infty} P(T = i\eta_2 + \eta_3)(i\eta_2 + \eta_3) \\ &= \sum_{i=1}^{\infty} a_{02} a_{22}^{i-1} a_{21}(i\eta_2) + a_{03}a_{31}\eta_3 + \sum_{i=1}^{\infty} a_{03}a_{32}a_{22}^{i-1}a_{21}(i\eta_2 + \eta_3) \\ &= \frac{a_{02}a_{21}\eta_2}{(1-a_{22})^2} + \frac{a_{03}a_{32}a_{21}\eta_2}{(1-a_{22})^2} + a_{03}a_{31}\eta_3 + \frac{a_{03}a_{32}a_{21}\eta_3}{(1-a_{22})} \end{aligned} \tag{9}$$

$$\begin{aligned} S &= \sum_{\forall j}\sum_{\forall i} P(T = (\eta_1 + i\eta_2 + j\eta_3)) \times T \\ &= \frac{a_{02}a_{21}\eta_2}{(1-a_{22})^2} + \frac{a_{03}a_{32}a_{21}\eta_2}{(1-a_{22})^2} + a_{03}a_{31}\eta_3 + \frac{a_{03}a_{32}a_{21}\eta_3}{(1-a_{22})} \\ &+ (a_{01} + a_{03}a_{31})\eta_1 + \frac{(a_{02}a_{21} + a_{03}a_{32}a_{21})\eta_1}{(1-a_{22})} \end{aligned} \tag{10}$$

Taking each FIFO as an M/G/1/K queuing system, the probability that there are m packets arrived during the time that one packet is processed can be calculated by (11):

$$k_m = \sum_{\forall T} \frac{(\lambda T)^m}{m!} e^{-\lambda T} \times P(T = \eta_1 + i\eta_2 + j\eta_3) \tag{11}$$

Making $a_i = k_{i+1} + k_{i+2} + ... = P\{m > i\}$. For an M/G/1 queuing system:

$$\begin{cases} \pi_0^{\infty} = 1 - \rho^{\infty} \\ \pi_i^{\infty} = \dfrac{1}{k_0}\left(a_{i-1}\pi_0^{\infty} + \sum_{j=1}^{i-1} a_{i-j}\pi_i^{\infty} \right) \end{cases} \tag{12}$$

Where $\rho^{\infty} = \lambda S$. Therefore, the steady probability that there are i packets in M/G/1 queuing system is:

$$\pi_i^K = \frac{\pi_i^{\infty}}{\sum_{i=0}^{K-1} \pi_i^{\infty}} \tag{13}$$

The utilization rate of FIFO and the average sojourn time of packet in local FIFO can be calculated through (14) and (15):

$$\rho = \lambda(1 - \pi_{K-1}^K)S \tag{14}$$

$$H = \frac{\sum_{\forall i} i\pi_i^K}{\lambda(1 - \pi_{K-1}^K)} \tag{15}$$

V. VALIDATION

In order to validate the proposed model, we build a simulation platform to test the utilization rate of FIFO and the average sojourn time of packet in local FIFO. For the utilization rate of FIFO, we compare the simulation results with the result obtained from our model. For the average sojourn time of packet in local FIFO, the simulation results are compared with the results obtained from our model and the results obtained from Jc H Model [23] (Note that Jc H model has the same router architecture and model assumptions with our model in this paper). For some related parameters in model, such as average packet insert rate, FIFO length, packet size, block probability of downstream FIFO and average service time of downstream FIFO, we choose some different values to validate the effectiveness of our model. For each assigned value, we run the simulation 50 times and compute the average value of the results.

A. The utilization rate of FIFO

Fig.3 show the FIFO utilization rate when (K=3,M=10,P_b=0) in the steady state. In Fig.3, Simulation means the simulation result got from the simulation platform, Model means the result got from our model.

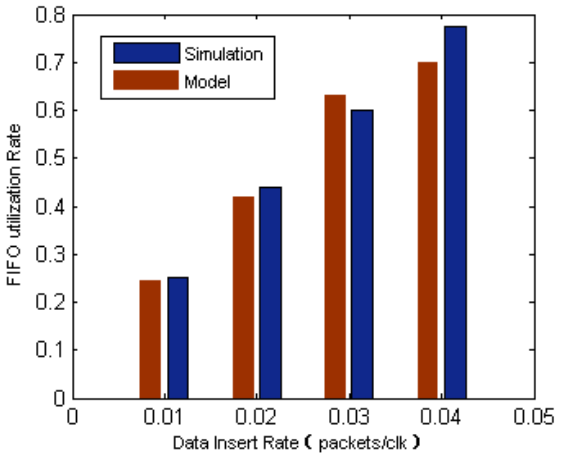


Figure.3 The utilization rate of FIFO when (K=3□M=10□P_b=0)

From Fig.3, we can get that our model can capture the utilization rate of FIFO when the downstream FIFO isn't blocked. Defining the relative error is (|Model-Simulation|/ Simulation), we can get the relative error is less than 10% in Fig.3.

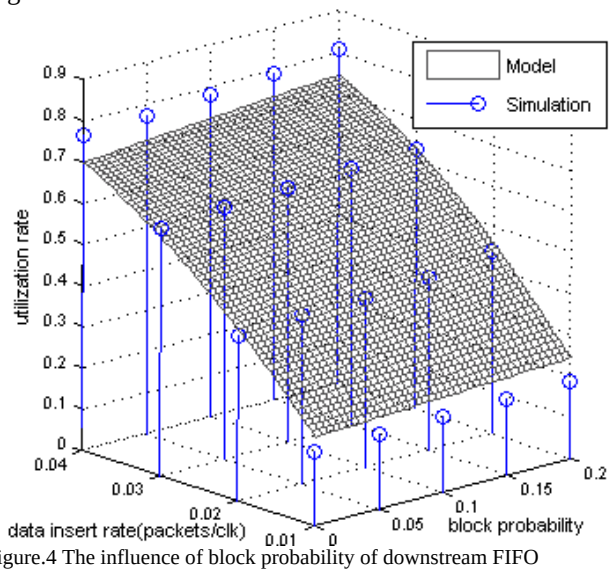


Figure.4 The influence of block probability of downstream FIFO

To evaluate the influence of block probability of downstream FIFO for our model, Fig.4 compare the simulation result and the model result for different value of P_b when K=3 and M=10. In Fig.4, Simulation and Model

have the same meaning with Fig.3. From Fig.4, we can get that our model is available when the block probability of downstream FIFO is changed and the relative error is less than 16%.

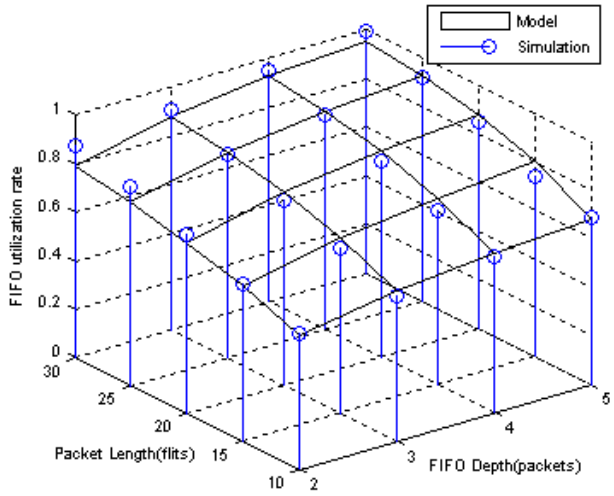


Figure 5 The influence of FIFO depth and packet length

To evaluate the influence of FIFO length and packet size, Fig.5 compare the simulation result and the model result for different value of K and M when P_b=0.01 and $\lambda = 0.03$. From Fig.5, we can get that our model can get the performance of FIFO for different values of K and M when other parameters in model are given, in this paper, we make $\lambda = 0.03$ and P_b=0.01, the relative error is less than 10%.

B. *The packet average sojourn time in FIFO*

In order to evaluate the effectiveness of our strategy, the simulation results of average sojourn time in local FIFO are compared with the results obtained from our model and the results obtained from Jc H Model. Fig.6 shows the comparison for different values of date insert rate and different values of block probability when K=3, M=10.

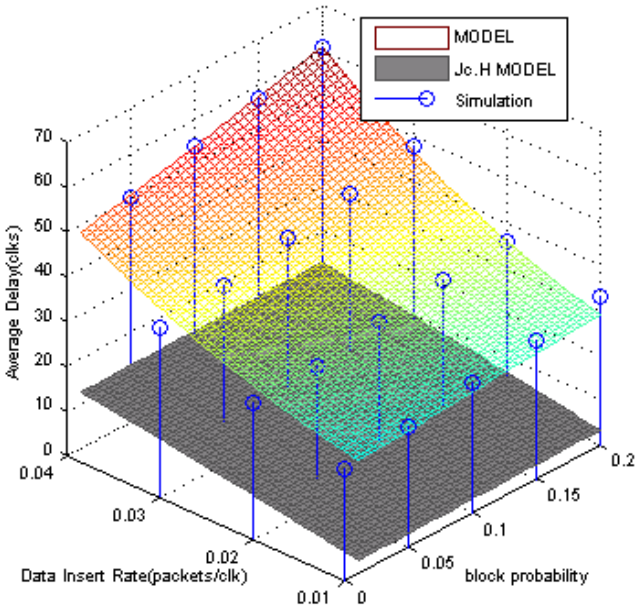
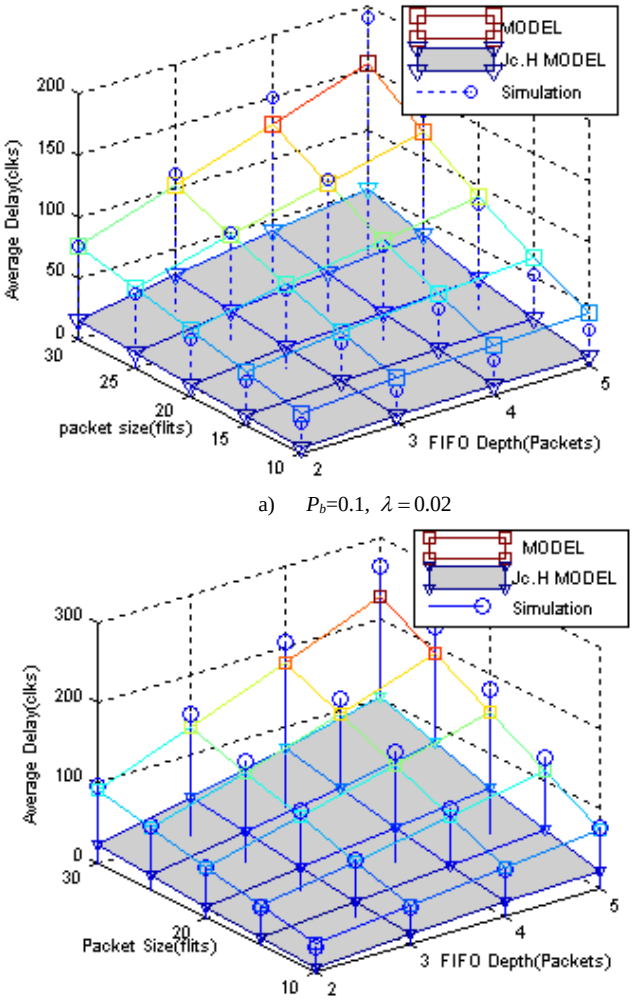


Figure.6 the packet average sojourn time in local FIFO when K=3, M=10

In Fig.6, Simulation and Model have the same meaning with Fig.5, Jc. H MODEL is the result based on the method in [23]. From Fig.6, we can get that our model can get the packet average sojourn time in local FIFO and the relative error is less than 19%. Moreover, the results got from our strategy are more close to the simulation results than Jc. H Model.

To evaluate the influence cased by the parameters K and M, some different values of K and M are chose for simulation. Fig.7 a) and b) show the comparison between simulation and two models in (P_b=0.1, $\lambda = 0.02$) and (P_b=0.2, $\lambda = 0.04$), respectively.



a) P_b=0.1, $\lambda = 0.02$

b) P_b=0.2, $\lambda = 0.04$

Figure.7 The influence cased by the parameters K and M

From Fig.7, we can get that our strategy is still available for different values of K and M, and the results got from our strategy are more close to the simulation results than Jc. H Model, too.

VI. CONCLUSION

A performance analytical strategy for Network-on-Chip router with input buffer architecture is proposed in this paper. Given the related parameters, the model can analyze schedule delay and the average service time for the local FIFO, and the data average sojourn time in a router can be calculated by using the model and the queuing characters of the buffers. At the end of the paper, we compare the results from our model with the simulation results and the results got from Jc H model to validate the effectiveness of our method. For the variable parameters in our model, we choose some different values to validate the practicability of our method. Because some approximations used in the progress of modeling in this paper, there are some errors between the analyzed results and the simulation results. To

reduce the errors need to intensive study of the SMP and the queuing system. However, the strategy in the paper could be still implemented as a useful tool to analyze the NoC router performance.

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