Controller Architecture Design for MMC-HVDC

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***Abstract*—Compared with high voltage direct current (HVDC), the primary and secondary systems of modular multilevel converter based HVDC (MMC-HVDC) are complicated. And the characteristics of the control system determine the properties of the MMC-HVDC system to a certain extent. This paper investigates the design of control architecture. First, the structure and parameters of the 21-level MMC-HVDC are designed. Second, the framework of the control system is studied in details and a complete control system is established. The communication mode and content are built between each layer, and the control system program is developed and debugged. Then The steady state test platform of the sub-module and the relevant control system are designed. Finally, the steady-state tests and the system test of the physical MMC-HVDC simulation system are conducted, which prove that the SMC can control the sub-module (SM) efficiently, and the control system could realize efficient start and stop of the physical system. Meanwhile, the capacitor voltage balance between the sub-modules and the basic fault protection and control of the DC voltage and power are verified to be effective.**

***Index Terms*—physical simulation system, modular multilevel converter (MMC), pole controller & protection system (PCP), valve based controller (VBC), sub-module controller (SMC), steady-state test platform.**

I. INTRODUCTION

Voltage source converter high voltage direct current (VSC-HVDC) has the advantage of quick and independent control of active power and reactive power, convenience in load flow reversing, and ability to supply power to weak ac system and passive ac system, which LCC does not possess [1]. Modular Multilevel Converter (MMC) is a new multi-level voltage source converter VSC topology [2]. High DC voltage is obtained by superposition of a number of sub-modules, which could avoid direct series press-packed connection of the semiconductor devices and hundreds of output voltage levels can be achieved. Compared with the 2- and 3-level VSC, the MMC output voltage harmonic contents and switching losses are reduced greatly and the voltage level can be changed flexibly [3-4]. In VSC-HVDC applications, the use of MMC topology has become an international development trend.

So far, studies on the MMC-HVDC mainly concentrated in its modelling, modulation and control strategies [5-13]. But almost no references did research on the design of MMC-HVDC physical simulation device or control systems. In Ref. [14] MOSFET is integrated with sub-module controller (SMC) in designing SM and CompactRIO is taken as pole controller & protection system (PCP) to design MMC-HVDC dynamic simulation device which is fit for research application. Ref. [15] introduces the designing and dynamic simulation method for valve based controller (VBC) and puts forward a capacitor voltage balance method. Ref. [16] and [17] mainly focus on the hierarchical structure of control system. Ref. [18] designs and develops hardware, software and protection strategy of VBC, which have already been applied in Shanghai Nanhui wind farm integration project.

MMC-HVDC physical simulation primary system is designed in this paper. Control system uses hierarchical controlled manner, from top to bottom the control system is made up of the interfacing computer (PC), PCP, VBC and SMC. System status information is received by the host computer via an Ethernet from PCP, and the needs of human-machine interface displays and real-time control algorithms are taken into consideration. To ensure the rapidity of the protection system, breakers are controlled by PCP directly and also operated by PC remotly. VBC communicated with SMC by a multiplexed pair of optical fibers for the asynchronous communication between VBC and SMC, which minimizes the number of optical fibers and reduces the complexity of the control system. A sub-module (SM) steady-state test platform is designed, and results of SM steady-state test show the validity of SMC and SM. MMC-HVDC system experiment results verified that MMC-HVDC physical simulation system can start and stop efficiently, active and reactive type valve changes can be achieved, SM capacitor voltage can be balanced, valve and AC system fault protection and other functions can be achieved.

I. MMC-HVDC PHYSICAL SIMULATION SYSTEM

A. MMC converter and SM structure

As shown in Figure 1, the MMC contains six symmetrical arms, and each arm contains N SMs which were connected with a reactor L in series. An upper and a lower arm constitute a phase unit.

The equivalent circuit of the MMC-HVDC rectifier system is shown in Figure 2. P & N represent positive and negative DC bus in the converter, with the pole to ground voltages $U_{dc}/2$ and $-U_{dc}/2$ respectively. Take phase A for example, U_{a1} and U_{a2} are the upper and lower arm controllable voltage sources, U_{ao} is AC side output voltag of phase A, formulas (1) and (2) can be obtained:

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$$\begin{cases} u_{a1} = \frac{1}{2}U_{dc} - u_{ao} \\ u_{a2} = \frac{1}{2}U_{dc} + u_{ao} \end{cases} \quad (1)$$

$$u_{a1} + u_{a2} = U_{dc} \quad (2)$$

From formula (1) and (2): the output voltage of converter can be adjusted by allocating the number of SMs in the inserted state of the upper and lower arms, and DC voltage can be maintained constant for the number of inserted SMs in 3 phase units are equal at anytime.

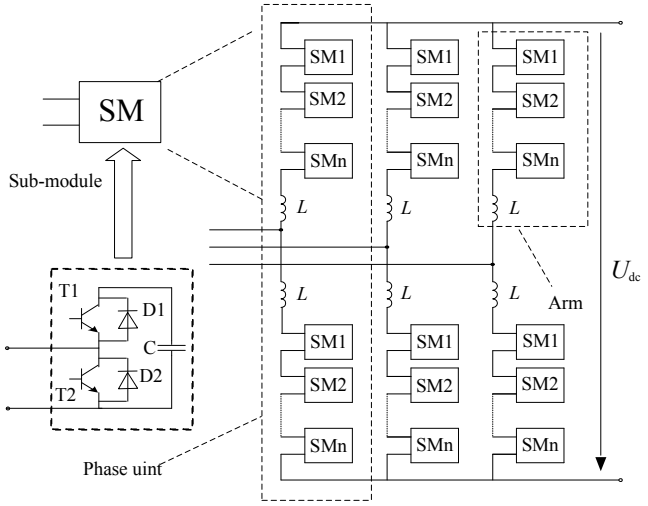


Figure 1. The topology of MMC

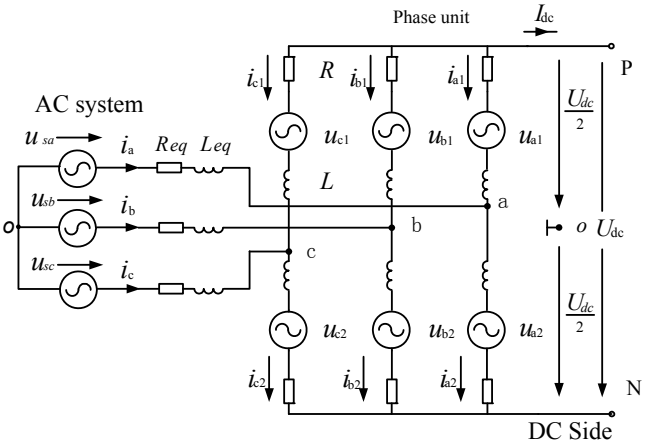


Figure 2. Rectifier sides model of MMC-HVDC system

If commutation reactor loss and harmonic components are ignored, take the rectifier side converter for example, active power P and reactive power Q between MMC and AC system are as follows:

$$P = \frac{U_S U_C}{X}\sin\delta \quad (3)$$

$$Q = \frac{U_s(U_s - U_c\cos\delta)}{X} \quad (4)$$

Here, U_s is the fundamental line to line RMS of the AC bus voltage, U_c is the fundamental line to line RMS of the converter output voltage, δ is the angle of U_c lags U_s, X is the equivalent inductance of commutation reactor L.

SM consists of two IGBT used as switches and a dc energy storage capacitor. A thyristor and a contactor are used as bypass switch. As shown in Figure 3, T1 and T2 represent IGBT, D1 and D2 represent the IGBT anti-parallel diode, C1 represents the DC side capacitor, S is mechanical bypass switch of SM, which can bypass SM for a long time, T is electronic bypass switch for fast protection of D2. And u_C is the capacitor voltage, u_{SM} is voltage across the SM, i_{SM} is the currents flowing into the SM, the reference direction of each physical quantity as shown in figure 3. According to switching states of T1 and T2, the state of SM can be divided into inserted, bypassed and blocked: (1) T1 is switched on and T2 is switched off, u_{SM} equals to u_C. In this state, the capacitor of SM is always accessed to the main circuit, which charge or discharge SM. (2) T1 is switched off and T2 is switched on, u_{SM} is zero. (3) T1 and T2 are blocked, this abnormal condition happens when SM capacitor is pre-charged for MMC starts or in the event of system failure to protect the converter.

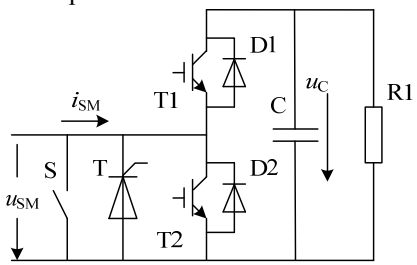


Figure 3. The internal structure of submodule

When the SM is transferred from inserted to bypassed state or from bypassed to inserted state, as characteristic of the IGBT are not identical, T1 and T2 may be switched on at the same time, so the capacitor is shorted. Therefore, it is necessary to set dead time for the two IGBTs, the setting method of dead time is adding blocked mode into the SM switching operation. After setting the dead time t_d, the relationship between the changes of u_{SM} and i_{SM} is shown in Figure 4.

1) "Inserted-bypassed" to "inserted-blocked-bypassed".If i_{SM} is greater than 0, error voltage appears, If i_{SM} is less than 0, no error voltage is generated.

2)"Bypassed-inserted" to "bypassed-blocked-inserted". If i_{SM} is greater than 0, no error voltage is generated. If i_{SM} is less than 0, error voltage appears.

The output voltage is distorted, the fundamental component is reduced, and the harmonic component is increased by the dead time. It is more difficult for arm current direction detection. However, in order to prevent the SM capacitor, dead time of the upper and lower IGBT is set in software in this paper.

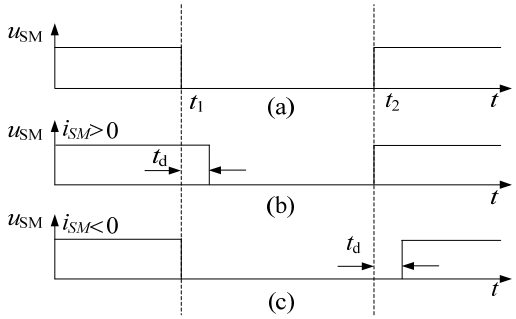


Figure 4. The output voltage of SM

B. Primary system of physical simulation system

The rated power of MMC-HVDC physical simulation system is 100kW, the rated DC voltage is ± 2kV. Rated DC current 25A, rated AC current 28.86A, over current

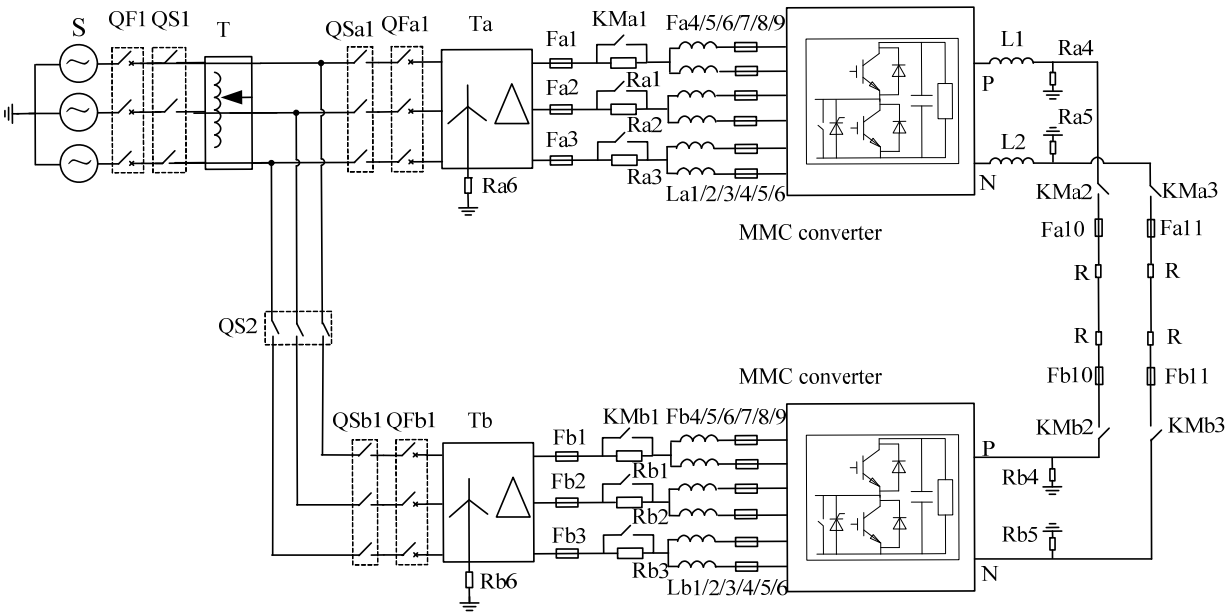


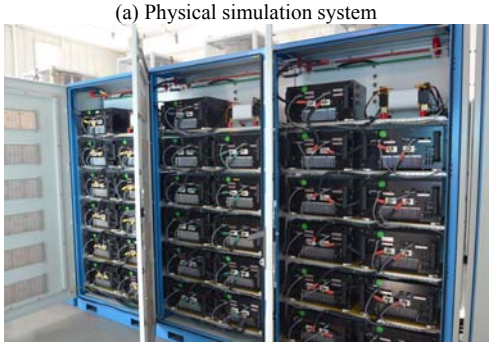
Figure 5. The primary system of MMC-HVDC physical simulation system

protection value 30A. Each arm of converter has 22 sub-modules, and of which two SMs are used as spinning reserve. Main circuit of physical simulation system is shown in Figure 5, the symbols have the following meanings:

S	AC system power source
QF1	Incoming line breaker
QS1, QS2	Incoming line disconnecter
T	Regulator
QFa1, QFb1	Breaker
QSa1, QSb1	Disconnecter
Ta1, Tb1	Converter transformer
Ra6, Rb6	Grounding resistors
Fa1-3, Fb1-3	Transformer secondary fuses
KMa1, KMb1	Hurl-slices switch
Ra1, Rb1	Current limiting resistor
Fa4-9, Fb4-9	Arm fuses
L1, L2	Smoothing reactor
Ra4, Rb4	Positive grounding resistance
Ra5, Rb5	Negative grounding resistance
KMa2, KMb2	DC positive pole swith
KMa3, KMb3	DC negative pole swith
Fa10, Fb10	DC positive pole fuses
Fa11, Fb11	DC negative pole fuses
R	DC line equivalent resistor

The rated input voltage of the regulator T is 380V, and the output voltage is raged from 0 to 430V. Rated capacity of converter transformer Ta and Tb is 120kVA, the transformation ratio is 0.38kV/2kV and the positive leakeage inductance of the transformer is 0.1 p.u.. There is 50% taps on ransformer secondary side, and transformer connection group can be changed with power off. Fuses are equipped in the converter transformer secondary side, converter arms and DC lines. Current limiting resistor is 50Ω, arm reactor is 20mH. Three-phase PT and single-phase CT is used in the main circuit. Active interfaces are reserved in the primary and secondary sides of the converter transformer and the DC side of the MMC-HVDC system, so the filtering and fault simulation could be increased according to the need. Resistor is used to represent DC line and 1MΩ grounding resistors are set at both beside ends of the inverter. 15mH smoothing reactors are added at one end of the positive and negative DC bus. MMC-HVDC physical simulation system is shown in Figure 6.

(a) Physical simulation system



(b) Three phase arm

Figure 6. MMC-HVDC physical simulation system

C. Hardware design of SM

As shown in Figure 7, two SMs are mounted side by side in a power unit. Two SMC cards are located at the top of the

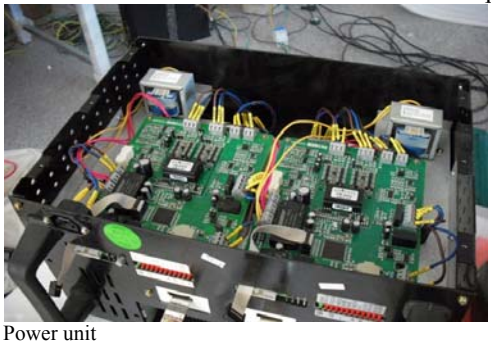


Figure 7. Power unit

power unit. The heat sink is located in the bottom of power unit. With front-in incoming line, primary connection port is located on the front panel centre of the power unit. SMC optical interfaces, LED indicator, J-Tag program download port are located on the front panel for the ease of experimental observation and operation. And 220V separate excitation single-phase AC power is adopted for SMC power supply.

II. CONTROL SYSTEM OF MMC-HVDC

Hierarchical control method is used in control system. PC displays primary system voltage and current signals, and controls active and reactive power. PCP receives reference value of active and reactive power from PC, calculates modulation ratio M and phase angle δ, VBC completes sorting of SM capacitor voltages and distributes trigger signals of SMs to SMC. SMC triggers SM and protects the IGBTs. PCP processing functions are jointly implemented by digital signal processor (DSP) and field-programmable gate array (FPGA). FPGA is also used as processor of VBC and complex programmable logic device (CPLD) is used as processor of SMC. MMC-HVDC physical Controller is shown in Figure 8. The hierarchical control system architecture is shown in Figure 9.

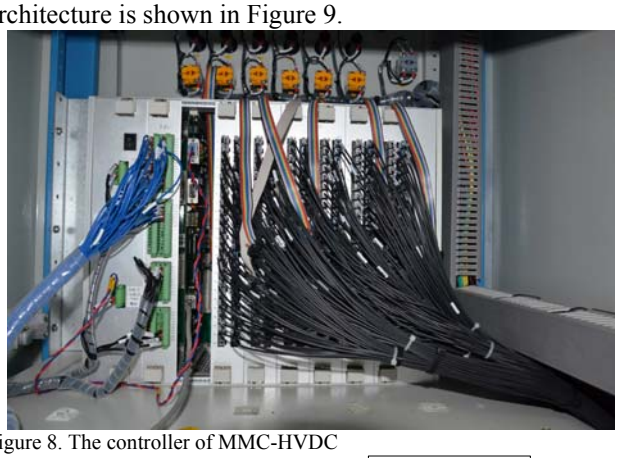


Figure 8. The controller of MMC-HVDC

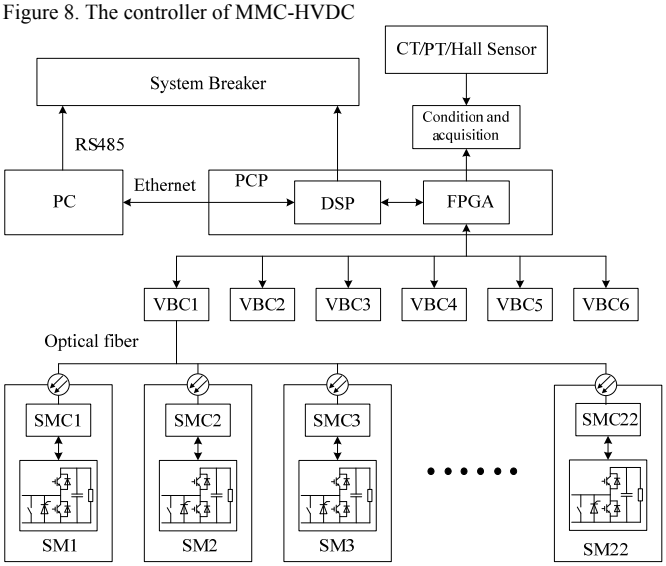


Figure 9. The architecture of control system

A. Communication between each control layer

Communication between each control layer is as follows:

1) PC to DSP: active and reactive power rate reference, proportional and integral time constant of proportional integral (PI) regulator, protection settings.

2) DSP to the PC: capacitor voltage of SM, SM status (over temperature, overvoltage, undervoltage, IGBT fault, communication fault), fault type of arm, operating parameters of primary system (current and voltage of transformer, arm current, DC voltage and current, active power, reactive power), the modulation ratio M and phase-shift angle δ, system status, arm fault signal.

3) DSP (PCP) to FPGA (PCP): reference of active and reactive power rate, protection settings, PI time constant.

4) FPGA (PCP) to the DSP (PCP): capacitor voltage of SM, SM status, fault type of arm, operating parameters of primary system, M and δ, system status, arm fault signal.

5) FPGA (PCP) to VBC: system status, the reference sine wave, the direction of arm current, synchronization signal.

6) VBC to FPGA (PCP): capacitor voltage of SM, SM status, fault type of arm, arm fault signal.

7) VBC to SMC: trigger signals of IGBT, mechanical contactors and thyristor, synchronization signal.

8) SMC to VBC: capacitor voltage of SM, SM status.

B. System operating states

Four operating states are set for the MMC-HVDC system: self-test, rectification, normal operation, and shutdown & emergency shutdown. The main purpose of self-test state is checking whether hardware and communication between all layers of control system is normal when the primary system is power off. Self-test procedure is as follows:

1) DSP issues a self-test command to the FPGA; PCP issued 16 bits self-test control word to VBC.

2) VBC contrasts whether the default 16 bits word is the same as the received control word, and communications self-test is done among all SMC which are managed by VBC to judge whether the SMC communication between VBC is correct.

3) The SMC self-test situation, validation of data received from PCP and self-test data sent to PCP are combined into 32 bits data, and then sent to PCP.

4) PCP receives 32 bits data, examines self-test word received from VBC and sends all the results to PC.

C. Interfacing computer (PC)

The monitoring and control function of the system are implemented by using Ethernet and RS485 communication. Various electrical quantities, status of breakers and disconnectors are displayed by PC quickly and accurately. The displayed parameters are comprised of three-phase voltages and currents of the transformer, active and reactive power exchanged between DC system and AC system, the captiator voltage of SM, the DC voltage and current. The voltages, current and power are sent from the controller via the Ethernet communication, using the MODBUS-TCP protocol to transmit to the upper interface. The displayed digital signal includes status of each breaker and disconnector, SM status and the type of fault.

In addition to display function, the PC can control breakers via RS485 remotly. The reference of active power and reactive power rate, time constant of PI regulator, the limit of M and δ, and the system protection value can be set in the control interface. Except the above function, PC can also record the historical curve of the various parameters.

D. Pole controller & protection system (PCP)

PCP processing functions are jointly implemented by the DSP and FPGA. Main function of PCP is depited in Figure 10.

The main functions of DSP are:

1) Receiving setting value and information of system status, sending information of SM voltage and status, information of the arm and primary system to PCP for ing on the interfacing computers.

2) Receiving information of SM capacitor voltage and status, arm and the primary system, generating modulation M and phase shift angle δ.

3) Sending values of reactive power and reactive power rate and PI parameters to FPGA for reference.

4) Processing primary system fault, and stopping the system in emergencies when transformer overvoltage or overcurrent, arm overcurrent, DC overvoltage or overcurrent fault occurs.

The main functions of FPGA are:

1) Acquisiting the voltage and current of transformer, the voltage and current of DC bus, the arm current.

2) Calculating active power, reactive power, DC voltage and the difference between the reference value of active and reactive power rate and the actual values, M and δ are calculated through PI regulator, forming a sinusoidal reference wave eventually.

3) Communicating with the DSP, receiving the reference active and reactive power rate, PI parameter; Sending SM status, voltage information, the arm information and primary system information to DSP.

4) Communicating with VBC, SM voltage, SM status, the arm fault information and fault signal are received form VBC, sending system operation status signal, the synchronous signal, the reference sinusoidal wave and the direction of arm current to VBC.

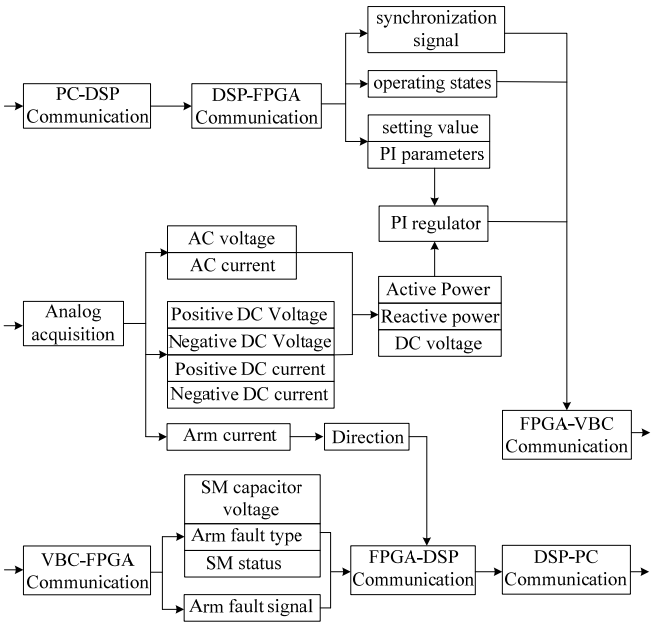


Figure 10. The program function of PCP

E. Valve based controller (VBC)

There are 24 pairs input and output VBC optical channels, communication speed of which is 5Mbps, and HFBR-1521ETZ and HFBR-2521ETZ is used as the fiber interface. Figure 11 is a schematic of VBC function.

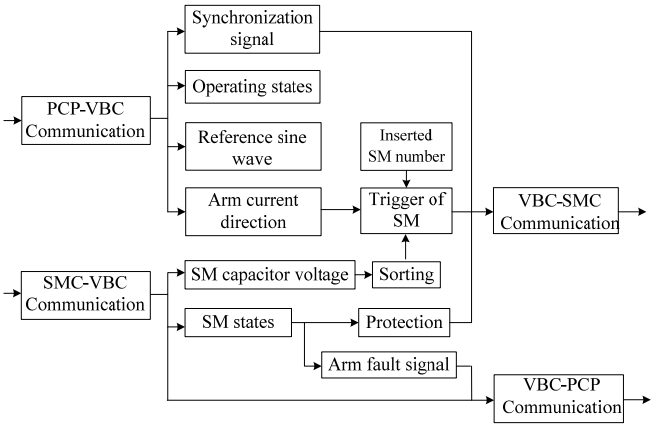


Figure 11. The program function of VBC

The main functions are:

1) Receiving the reference voltage of sinusoidal wave, current signal of arm, the state signal of the system from PCP; uploading capacitor voltages of SMs and the status signals of SMs to PCP.

2) Receiving reference voltage of sine wave from PCP, using nearest level control (NLC) to determine the opening number of an arm. The capacitor voltage of SMs received from SMC will be sorted only if conducting SM numbers in two adjacent periods are different. Based on the sorting results and the arm current direction, the SMs to be inserted and blocked are selected, in this way fluctuation range of SM capacitor voltage of SMs meets certain homeostasis.

3) Receiving the status signal from SMC, determining whether bypassing the corresponding SM according to the control strategy or not. The corresponding SM will be bypassed and the redundancy SM will be inserted When SM fault number of the arm is less than or equal to two. A fault signal will be uploaded to PCP via the backplane of the control cabinet when the fault number of SM is greater than two, and the open number of SM in the last control period will be kept before the PCP control the shutdown of the entire system.

4) Communicating with SMC, the IGBT signal, thyristor trigger signal, mechanical bypass contactor signal are composed of 8-bit control word to distribute to the SMC.

5) Ensure 22 SMs are triggered synchronously in the arm, which is achieved by sending synchronization singal to SMC in the beginning of each control cycle. Serial asynchronous communications is adopted between VBC and SMC through optical fiber. Operation circle is determined by a counter respectively in VBC and PCP, and introductions are operated at a certain point of the circle.

F. Sub-module controller (SMC)

SMC is responsible for SM voltages acquisition conversion and SM status monitoring, and sending information to VBC. Control information is received simultaneously from VBC to control IGBTs, and dead time of the two IGBTs is achieved in software. Mechanical bypass contactor and electronic thyristor are controlled by SMC. Hardware architecture of SMC includes AC power source, control chip, optical fiber, IGBT trigger voltage sampling and AD conversion, electronic bypass and mechanical bypass trigger, fault detection. Software features as the following Figure 12.

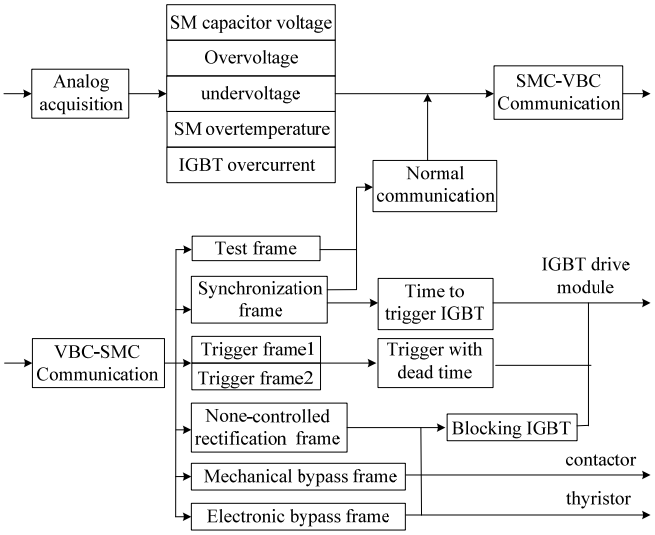


Figure 12. The program function of SMC

12 bits voltage of SM capacitor, overvoltage, and undervoltage, overtemperature and overcurrent signals of IGBT are collected by SMC to constitute a 24 bits control word and the control word is uploaded to VBC. 8-bit synchronous word and 8-bit control word are recevied from VBC data, including:

1) SMC synchronous signal: ensure synchronization of all the SMs, a control cycle starts after SMC synchronization signal is received.

2) System status: SMC can take appropriate actions in different operating conditions, such as blocking converters, blocking SM for undervoltage protection.

3) Test frame: when system is in self-test state, communications test data is sent from VBC to SMC. When self-test communication is completed, VBC downlink data will become the control information.

4) IGBT trigger frame: when the system is in rectification or normal operation state, two trigger signals of IGBT are sent from VBC to SMC. After dead time of the IGBT between trigger signals is added by SMC, IGBTs are triggered.

5) Electronic bypass signal: When it is necessary to bypass the SM or the system needs to shutdown, triggering the high-speed thyrister of SM for protection.

6) Mechanical bypass signal: When the SM fails, VBC confirms and makes mechanical bypass operation, and SM is bypassed from the main circuit.

There are two types of SM fault: communication fault of SMC and internal fault of SM.

1) Communication fault of SMC

Communication fault detection module detects the faults of received data, which includes overtime, the frame format error, and parity check error. Receiving data overtime refers to none of data or only a synchronous frame without any control frame is received in a control period. When receiving data overtime is detected, the fault is reported to VBC. Receiving frame format error means received data frame format of SMC does not match any normal frame. After a communication error is detected, fault is reported and the fault number is counted. SMC uses the correct control frame of last period for SM control.

2) SM internal fault

After the control system is powered, SM status is monitored. Capacitor voltages of SM are detected via SMC analog circuit. To prevent protection malfunction, SMC detects the start time of overvoltage or undervoltage, the fault is confirmed only if the abnormal condition last for a certain time. Else, fault is ignored. Overtemperature is achieved through the thermostat switch. Temperature switch is closed when overtemperature fault ocurrs, so voltage level is changed to high by the conversion circuit to send fault to processor. When the IGBT overcurrent fault occurs, IGBT is blocked by drive module quickly, and fault signal is sent to the processor.

At the start of one control period, capacitor voltages of SM and SM status will be uploaded to the VBC, which will send control information to the SMC before the end of the control period. If a SM fails, the fault information in a period initial stage will be uploaded to the VBC, which will receive all fault information to determine whether the number of failed SM is less than the number of redundancy SM. If number of failed SM in the arm is less than or equal to two, bypass the corresponding SM, and insert redundancy SM, If the number of failed SM is greater than two, upload a fault signal to PCP, and keep the open number of SM in the last control period before the PCP control the physical simulation system to stop. VBC sends stop request to the PCP, and PCP sends a stop command to the VBC. After receiving the stop command VBC to block all the SMs. Taking the VBC request to PCP the stop instruction time into accounts, SMC will receive control instructions of VBC in the next control cycle, and maintains the cycle state before stop instruction. When the SM fails, the control system can deal with failure in two control period.

Under the coordination control, the MMC-HVDC can run at a stable state, with fixed DC voltage, fixed active power, fixed AC voltage and fixed reactive.

III. SM STEADY-STATE TEST PLATFORM

A. Primary system of test platform

SM steady-state test platform consists of adjustable DC voltage source, a current limiting resistor, the DC capacitor and two IGBTs with anti-parallelled diodes. Test platform connect with the measured module through the right port, between which are the reactors. Since two SMs are packaged as a power unit, the two SMs are simultaneous measured in series. Figure 13 depicts the primary system of steady-state test platform.

Test platform and two SMs IGBT are controlled by SPWM, in which the test platform signal Tp1 and measured SM signal T1, T3 are the same; Tp2, T2 and T4 of measured SM control signal are the same. Two groups of signals are contrast.

When steady-state test platform is unloading, the test platform port output square wave. When TP1, T1 and T3 are switched on, the output voltage of the test port is U_t, otherwise when TP1, T1 and T3 are switched off, the output voltage is 0. After effection of smoothing reactor, the load current is sine wave with high frequency harmonics.

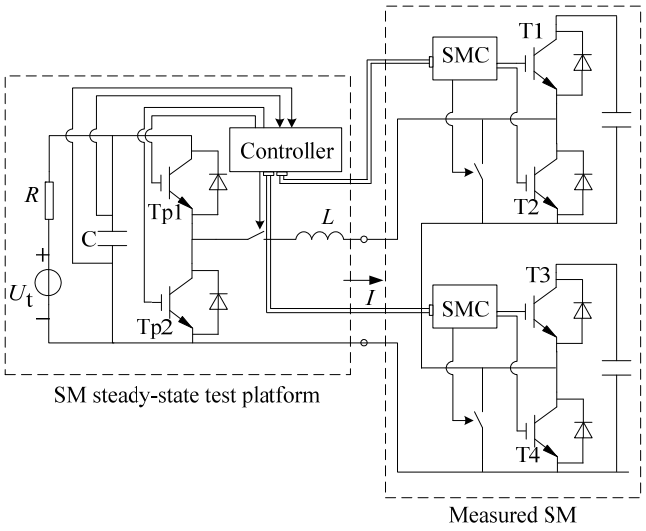


Figure 13. The primary system of SM steady-state test platform

B. *Controller design of test platform*

The controller of steady-state test platform not only controls IGBT triggers of the test platform, but also controls the IGBTs of measured SM. In order to meet different testing requirements of SM, different load currents can be adjusted by regulating DC power supply output voltage and SPWM modulation.

A custom serial communication protocol is adopted for test platform controller to communicate with the measured SMC. IGBT trigger signal, bypass signal and other information are sent to SMC, which will then send capacitor voltages and SM states back. Communication data is exchanged between test platform controller and measured SM with a fixed period.

To protect the test platform and SM, basic protection functions are added in the steady-state test platform software. Processor detects IGBT overcurrent fault, and then blocks IGBT, and cut off the load side switch. When the current of IGBT or temperature of SM overruns, the fault signal is received and uploaded to the test platform controller. The load side switch is turned off after receiving the fault signal, in order to protect the test platform and SM.

IV. Experiment Results

A. *SM steaty-state test*

Voltage of DC source U_t is regulated and the oscilloscope is connected to the output of the SM test platform to measure the output voltage. The experiment result is consistent with theory, and by adjusting the control button of the test platform to change SPWM modulation, the output voltage waveform modulation can be changed accordingly. Switch on the load side, gradually increase U_t, SM capacitor voltage and test platform voltage, and RMS of load current are displayed on the LCD screen of controller. The load current which is sine wave with high frequency harmonics and voltage waveforms of the measured SM are observed by oscilloscope.

B. *System experiment*

None-controlled rectification is adopted for SM capacitor charging. Unlock the trigger signal when the capacitor voltage of SM reaches a certain value by fixed DC voltage control. In the SM capacitor charging process, fixed AC voltage and DC voltage control are used in both ends of the converter.

Figure 14 shows a steady DC voltage waveform at 4kV. Figure 15 shows transformer primary voltage and arm voltage. Measured by the oscilloscope, RMS value of transformer primary voltage is 219V; the arm voltage has large harmonic content which is impacted by dead time of SM trigger signals to a certain extent. Figure 16 depicts capacitor voltages of 22 SMs in upper arm of phase A when the system is stable and DC voltage is 4kV, the capacitor voltages are balanced at about 200V.

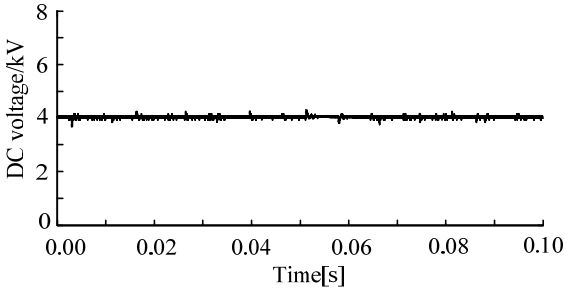


Figure 14. DC voltage

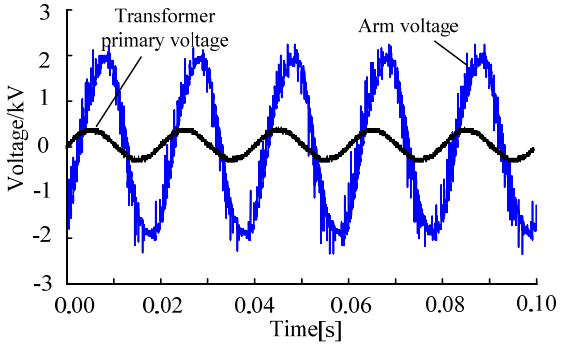


Figure 15. Transformer primary side voltage and arm voltage

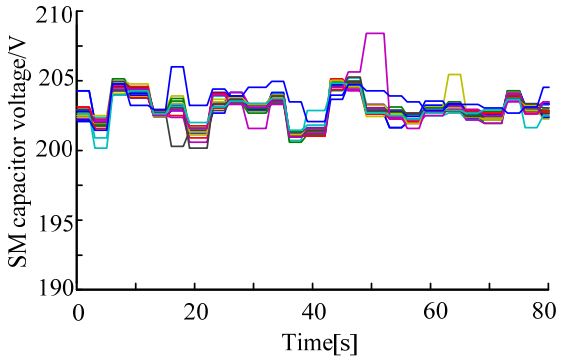


Figure 16. Capacitor voltages of upper arm in phase A

When the MMC-HVDC system startup process is completed, fixed DC voltage and reactive power control is used in the sending end converter, meanwhile fixed reactive power and active power control is used in the receiving end of the converter. Figure 17 and Figure 18 respectively display positive direct current and the current power when the DC voltage set value is 3kV and the active power set value is 65kW. Positive DC current is 20.1A, DC power is 60.7kW, and the 4.3kW less than the set values 60.7kW is the loss of double-ended converter stations, transformers and DC resistance.

When power drops from 60kW to 0, the DC power waveform is shown in Figure 19. Figure 20 shows the DC voltage wave form, as could be seen from the figure that there is no obvious variation of the DC voltage, which could prove the control effect of the system.

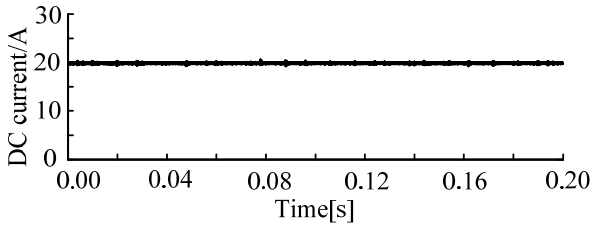


Figure 17. DC current of positive pole

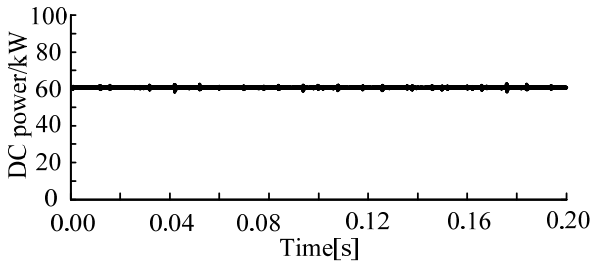


Figure 18. DC power

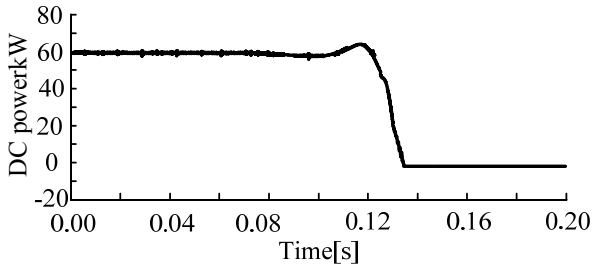


Figure 19. DC power when power drops

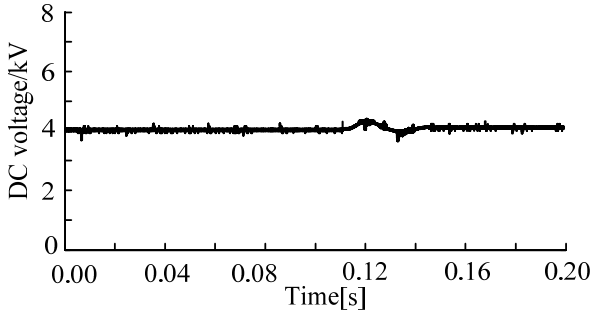


Figure 20. DC voltage when power drops

From the above experimental results, self-excited start, SM capacitor voltage balancing, and active power and DC voltage controlled can be achieved effectively in MMC-HVDC physical simulation system.

V. CONCLUSION

The architecture of control system is studied in this paper. Programs of the control system is developed and debugged, and the SM steady-state test platform and MMC-HVDC physical simulation system are established. Experiment is done to test performance of the system. The conclusions are as follows:

1) Hierarchical control architecture is adopted for control stystem which is divided into PC, PCP, VBC and SMC. MMC-HVDC physical simulation system can start and stop effectively. The DC voltage, active power, reactive power and AC voltage are well controlled. Capacitor voltage balance is achieved.

2) The hardware and software of steady-state platform is reasonablely designed, which can ensure the efficient of SM test. The steady-state operating characteristic of SM is examined, which can verify the correctness of the SMC and SM.SM steady-state test platform provides a quality detection methods of for setting production of many SMs.

3) MMC-HVDC physical simulation system can provide research platform for different control strategies of VSC-HVDC analysis and the development of new principles.

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