Design of Crosstalk Prevention Coding scheme based on Quintuplicated Manchester error correction method for Reliable on chip Interconnects

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***Abstract*—A low power Manchester based error-control code for on-chip interconnection-link has been proposed in this paper. It has a capacity to rectify nonuple errors of random and burst using standard N-Modular Redundancy (N-MR) error correction scheme. Manchester based Rectification of Single Error, Identification of Double Error(M-RSE-IDE) extended-Hamming code, and Quintuplication error correction scheme serves as the backbone for the proposed technique. Besides, both handle different tasks simultaneously. The former prevents the crosstalk of the interlinked-wire with the reduction in the coupling capacitance while the latter consumes less power by transiting data at the center of the bit. A new nonupler-decoding algorithm has put forward in the proposed Quintuplicated Manchester Error Correction (QMEC) to correct nine errors. Different analysis of reliability, area, power, delay and residual flit-error rate; interlink-swing voltage and interlink-power consumption of the designed QMEC code has been performed. The QMEC codec, when running with Manchester, counteracts nonuple errors with 25% of power reduction compared to QMEC without Manchester. QMEC not only outlined other existing error control codes by area and power but also reduced link-swing voltage and link power upto 91% and 85% respectively.**

***Index Terms*—codecs, error correction codes, system-on-chip, redundancy, reliability.**

I. INTRODUCTION

The latest integration to the Deep Sub-Micron (DSM) system is the VLSI technology and its emergence outperformed System on Chip (SoC). As SoC no longer accommodate the process elements leaving an overhead to overall system efficiency [1]. Networks-on-chip (NoC) is an innovative tactic to achieve a much higher degree of integration in a System on-chip. The Routing elements interconnect the processing elements with each other in NoC while the routing elements are interconnected through interconnection link [2]. Delayed transition, excess power consumption, and reliability are the critical issues for many researchers in the on-chip communication links of NoC of because of the technology nanometer regime [3]. Technology scaling has its other side as the communication delays in global interconnect than traditional logic gates. During the charging and discharging of the large interconnect capacitance, on-chip interconnect links consumed the major portion of the total chip power during a transition period. In addition, the reliability of interconnects and the routing elements depend on various factors especially the imperfections due to manufacturing [4] or a various noise origins such as environmental variation [5], coupling of Crosstalk [6,7], transit voltage fluctuations [8], process variations [9], thermostat variations [10], Electro Magnetic Interference (EMI) [11] and/or computation of these origins. On-Chip interconnects links weakened by all the above factors and are prone to more random and burst errors. Hence, the reliability of on-chip interconnects is increased by a new technique that reduces crosstalk with less power consumption has to be proposed that detects and corrects the errors.

To enhance the reliability with less power consumption, it is obvious that many researchers focused on power consumption by designing codes in a different format [12]. The above is achieved by reducing the switching activities of the fault type at runtime [13], which literally consumes less power. The earlier proposed codes were able to avoid crosstalk, can correct up to three-bit errors [14-17] and detect four-bit errors [18]. Later a work carried out by [19], proposed a code that could correct five errors.

A novel technique namely QMEC method had been proposed that is capable of correcting nonuple errors when compared to the previously proposed codes, which can correct a maximum of five-bit errors. The proposed code concentrates on the power consumption and reliability issues in NoC interconnect link. It reduces the crosstalk whilst correcting random and burst errors. The remaining of the paper is arranged as follows: Reliability of NoC Inter-connect links as related work in Section 2. In chapter 3, discussed the proposed Cipher and Decipher design, while in chapter 4, performance evaluation is presented. Eventually, Section 5 represents the conclusion.

II. RELATED WORK

Earlier many research associates focused on the codes that can correct up to one or two-bit errors using simple techniques such as Cyclic redundancy codes (CRC), Hamming Codes and Duplicate Add Parity (DAP) [3,14]. In general, these techniques were widely implemented in on-

Digital Object Identifier 10.4316/AECE.2018.04014

chip interconnects, which does not perform well due to data overloading. As a result, these approaches were effective against either random or burst errors separately at the cost of power while losing its efficiency in correcting both together. In order to overcome such issues and to handle multiple errors along with cross talk avoidance, have been developing new technologies to commute along with NoC in which different researchers have been performing their researches using a different coding scheme to enhance its reliability and performance. NoC widely incorporates Forward Error Correction (FEC) and Automatic Repeat request (ARQ) to provide in on-chip interconnect links to enhance reliability bound [20]. A development in the above, in [21] researchers highly focused on low and high noise environments and studied the impact of the same using adaptive error control schemes to reconfigure the code. This reconfigured code at minimal noise environment corrects only one random error and multiple random errors at high noise environment. The authors discussed performance in an AMBA bus-based system of single error correction and multiple errors detecting Hamming Codes as well as cyclic codes in [14].

In addition to the above, techniques involving low power such as Low Power Coding (LPC) has been proposed for on-chip buses power reduction [15]. In the past, researches carried out focusing on error resiliency but also looked into crosstalk interruption, as another issue. In lieu with the above, the authors[22] developed a simple error correcting scheme, single error correction codes (CAC/SEC) to minimize crosstalk interruption in the interconnection link and also corrects single errors while simultaneously detects double errors. To make the system resilient, different crosstalk avoidance codes such as the DAP [3] or Dual Rail (DR) code [16], Boundary Shift Code (BSC) [17], Modified Dual Rail Code (MDR), triplication error correction scheme [23] and Multi-Bit Random and Burst Error Correction code with crosstalk avoidance (MBRBEC) [19] are coupled with FEC scheme. The switching Capacitance associated with crosstalk reduces with FEC scheme from $(1+4\Upsilon)\ C_T$ to $(1+2\Upsilon)\ C_T$. In [24], two-bit burst errors were detected using proposed crosstalk avoidance SEC and these errors are corrected by using Hybrid ARQ (HARQ) retransmission scheme. In [34], proposed Penultimate Subtracted Fibonacci (PS-Fibo) crosstalk prevention coding scheme completely removes Triplet Opposite Direction (TOD), which is the main cause of crosstalk by numerical method. In [18], the author put forward the error correction scheme such as Triple error correction and quadruple error detection scheme using DAP. In [23], to rectify only one single random error, authors projected triplication error correction coding scheme. Many researchers have been working to make the research more logical and effective. In this regard, authors have been trying to incorporate the change in the coding scheme with effective utilization of hardware redundancy to carry out different possibilities.

According to [25], it is evident that there is a link between the theory of Error Control Codes (ECC) and incorporation of hardware redundancy for fault tolerance. In [26], the authors have proposed an indicator model to analyze the reliability issues of N-MR systems in faulty environments. As quoted in [27], to alleviate the failures of two memories in the same period and position, Triple Modular Redundancy (TMR) design is not sufficient. Hence, the author proposed Nine Redundancy (NMR) that deciphers to solve the TMR problem at the cost of resources. The Five Modular Redundancy (FMR) with Mitigation Technique was implemented to full-fill the gap between TMR and NMR in [28]. According to [29] Single event upset (SEU) error is alleviated by TMR. To achieve better reliability, SEU errors are tolerated by the newly developed Quintuple modular redundancy (QMR) system [29]. Hence, QMR system is more reliable under significant and necessary conditions compared to TMR. From the above discussion, a new coding scheme Quintuplication from QMR system has been identified that rectifies up to nonuple errors with crosstalk avoidance.

Researchers have also explored other research areas in order to improve power utilization and came up with coding schemes such as Manchester encoding. In [30], to solve the reduced swing problem the researchers have proposed a programming technique based on two-level Manchester encoding that utilizes the power efficient circuitry appropriately. In [31], for better DC balancing, FM0 and Manchester Encodings plays a vital role and improves the reliability of the signal. The constancy in the signal by DC balancing is improved with the help of Manchester and FM0 encoding [35]. From the above research, DC balancing can utilize Manchester encoding for the power reduction as it improves the signal level.

In the previous research, most of the authors have focused in correcting multiple errors and landed in five errors. As an advancement in this a new coding scheme, Quintuplication with Manchester coding scheme known as QMEC that combines the effectiveness of correcting nonuple errors by consuming less power.

III. Crosstalk Prevention Based on Proposed QMEC

Because of technology scaling, crosstalk is one of the major source for random and burst errors. $(1+4\Upsilon)C_T$, serves as the absolute capacitance of on-chip interconnection link, where the proportion of the coupling Capacitance to that of bulk Capacitance is represented by Υ, while the output load Capacitance is represented by C_T. According to [32], coupling capacitance of links was determined by the transition of data on adjacent wires. When the transformation of the two neighbors with respect to the victim wire occurs in the direction opposite to the flow, leads to the worst-case crosstalk [19].

In the interconnect wires, due to the integration of Crosstalk Prevention Codes (CPC), the worst-case Capacitance decreases from $(1+4\Upsilon)C_T$ to $(1+2\Upsilon)C_T$. As an outcome of coupling capacitance reduction, the CPCs reduces the dissipation of energy per path in a NoC link [18]. Though logically the avoidance of crosstalk is explained as above, it is much more important to achieve practical and is done by making as a vital component of any error rectification methods.

To avoid crosstalk schemes, the proposed duplication method and duplication with two-fold approach [18] have been ripped out by triplication-error correction scheme that corrects up to five errors [19]. In this paper, a simple and reliable concept with a combination of Quintuplication and

Manchester Error Correcting Scheme, known as QMEC code that corrects nonuple errors has proposed. QMEC coding scheme accomplishes the dual task of reducing crosstalk and enhances the resilience against random and burst errors effectively by consuming less power.

A. Model of the Proposed QMEC Cipher

Designing of the Cipher is vital, as the transition of data has to flow flawlessly. In this regard, the data bits are encoded by the proposed QMEC Cipher with the help of Manchester-based RSE-IDE extended Hamming code (39, 32). For the information to flow flawlessly, first, the information bits, say 'k' in number is encoded by RSE-IDE extended Hamming code. The encoded bits 'n' then passes through the Manchester Cipher where it further stabilizes the logic 0 by 0 to 1 transition while 1 to 0 for logic 1 at the center of the bit [30, 31]. When the data is manchesterly encoded, the data transmission occurs only at the center of the bit by reducing the encoded data into a half, which is the significance of it. The DC component of the signal carries no information but transmits the data successfully without carrying power [35]. The encoded data transition occurs through the on-chip interconnect link and during this, the errors are rectified by the proposed quintuplication. The mechanism of QMR is incorporated in quintuplication that enhances the data error correction [29].

Each encoded 'n' bits are quintuplicated resulting in '5n'. For instance (n,k) is the initial value of RSE-IDE then the final outcome bits are 2n+1. For example, let us consider 32 bits as the original input then after encoding with M-RSE-IDE (39, 32) extended Hamming code becomes 39 and 195 after quintuplication with a parity bit. Thus QMEC is a (195, 32) coding scheme for 32 bit wide data. Before the quintuplication of the encoded message, the lowest Hamming Distance of the Manchester based RSE-IDE extended Hamming code is 4, while after the minimum Hamming distance increases to 20, which provides an insight about the error correction accordingly.

According to the coding principle, the lowest Hamming distance of 't' can rectify errors. Henceforth, QMEC code corrects up to nonuple errors with the effective coupling capacitance of $(1+2\Upsilon)C_T$. Fig.1a represents the proposed QMEC Cipher block diagram while Fig. 1b represents the flow diagram. The above proves that QMEC has the higher transient error resilience along with the similar crosstalk characteristics.

B. Model of the Proposed QMEC Decipher

In a cyclic movement, an encoded bit has to be decoded with the proposed QMEC Decipher. The design of the M-RSE-IDE Decipher is depicted in Fig. 2. The order of decoding has to follow a systematic flow of the RSE-IDE Decipher, which is a syndrome computation pattern that corrects the single error and detects double errors.

The QMEC Decipher works in M-RSE-IDE model that detects and corrects up to nonuple errors after decoding. If the value of syndrome is not zero during the occurrence of nonuple errors, then the errors will be deducted by RSE-IDE Decipher while alternatively if the Decipher doesn't detect nonuple errors then the value of the syndrome is zero. QMEC decipher's nonuple algorithm is shown in the flowchart Fig. 3 and is explained as follows.

i. The encoded data are clustered as ctr_A, ctr_B, ctr_C, ctr_D and ctr_E in a cluster splitter.

ii. The cluster splitter is an inter leaver that splits the encoded data in to five received cluster data named as Rx_A to Rx_ E.

iii. The five received clusters are allocated to their respective Manchester RSE-IDE Deciphers that calculates the values of syndrome as SDE_A, SDE_B, SDE_C, SDE_D, SDE_E and appearance of double errors as DoE_A, DoE_B, DoE_C, DoE_D, DoE_E for the five clusters.

iv. Each RSE-IDE Decipher rectifies the appearance of single error while identifies the appearance of the two errors in each cluster with respect to their syndrome value.

v. Each encoded data after decrypting are transmitted to the selection switch as DCRT_A, DCRT_B, DCRT_C, DCRT_D and DCRT_E.

The Cipher and the Decipher of the QMEC scheme utilize XOR gates as Manchester logic. The S1, S2, S3, S4, S5 and S6 are the syndrome values calculated from the received data in the syndrome computation block. The syndrome decrypted unit deducts the error location of single error for the given syndrome values and its inverted values using AND trees. XOR gates that serve as the point of correction carry out the adding of error vector to the decoded codes. At the point of double error detection of the extended Hamming Decipher, an even parity of syndrome parity bit serves as the indicator for the entire encoded bits. The even parity bit of zero value check determines errors with zero or even numbers, while the other non-syndrome bits indicate the occurrence of at least an error.

The extended Hamming code finitely detects up to two errors only thus leading to an assumption of double errors only. The message decrypter separates the 39 bits into 32 information bits those includes 7parity bits and 32 encoded bits. Syndrome values and the overall parity bit detect the double error bit. The above mechanism

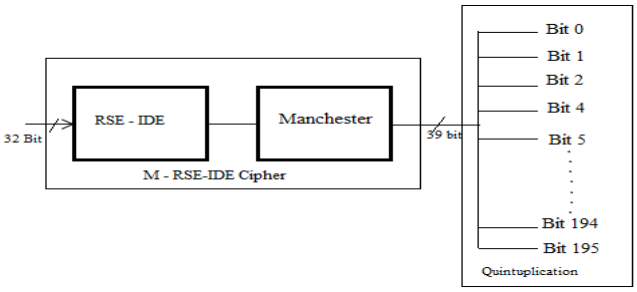

Figure 1a. Block diagram of QMEC Cipher

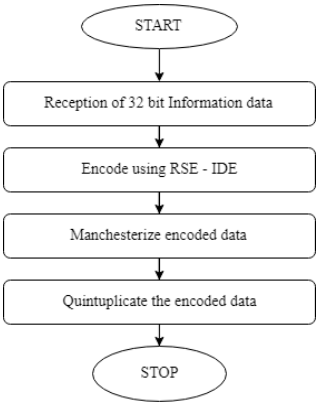

Figure 1b. Flow diagram of QMEC Cipher

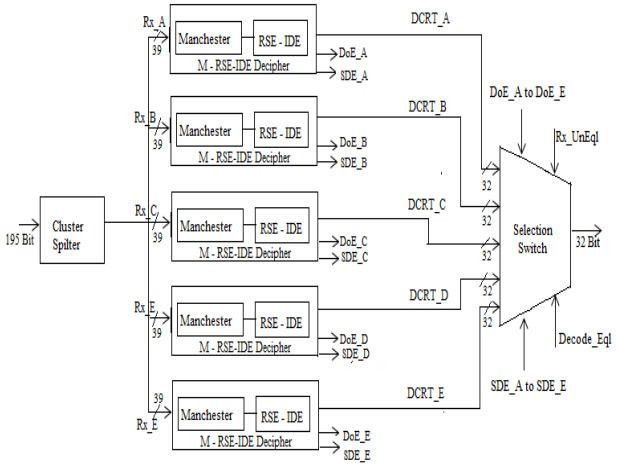

Figure 2. Block diagram of the QMEC Decipher

seems to be familiar while the decoded bits from the Manchester RSE-IDE pass through selection switch that comprises nonupler algorithm to correct nonuple errors

C. Measuring Reliability

Reliability is the measurement of the probability of Decipher error or failure [20]. The reliability of the chip depends on the voltage disturbances that are due to noise environment from many origins. In a basic model projected in [19-20] depicts the probability of error when a transition occurs in a single wire. The below eqn. 1 explains the probability of error,

$$\tau = Q\left(\frac{V_{SW}}{2\sigma N}\right) = \int_{V_{SW}/2\sigma N}^{\infty} \frac{1}{\sqrt{2\pi}} e^{-z^2/2dz} \quad (1)$$

Where V_{sw} is the inter link-swing voltage and σ_N is the predictable difference of the noise voltage, which is of a normal distribution. It is assumed from eqn. 1 that in each wire the probability error is unbiased irrespective of the data. Due to phenomenal technology growth, the density of the wire is increased accordingly this may transmit the data to the desired location promptly but are liable to random and burst errors largely. The above scenario leads to a maximum possibility of occurrence of multi-wire burst errors when compared to the possibility of multiple wire random errors in the adjacent wires [19].

A more realistic error design spatial burst error overcomes the deficit of calculation. Remodeling of error model represented in [1] includes burst error. The remodified noise source model affects the neighbor wire rather than affecting single wire. A coupling probability, Pc (0≤Pc≤1) describes the effect on neighboring wires [20]. Increase in Pc, indicates that it is directly proportional to errors of the neighboring due to the noise head [20]. If Pc is considered a probability of errors, the probability of single data error is represented as eqn. 2.

$$P(x=1) = (1-P_c)^2 \tau \quad (2)$$

where τ is explained in eqn. 1. Let us consider the possibility of 2 and 3-bit errors that are rooted by corresponding multiple noise heads P (x=2) and P (x=3) are depicted in eqn. 3 and eqn. 4.

$$P(x=2) = 2P_c(1-P_c)\tau \quad (3)$$

$$P(x=3) = P_c^2 \tau \quad (4)$$

The probability that l_{n+2} and l_{n-2} influenced by the same noise head 'l_n' is very less than P_c. The possibility of noise heads with greater than or equal to four burst error is ignored due to less probability P(x=4) / I_n=0 [19].

1) Residual Flit Error of the Proposed QMEC

As mentioned earlier in the measurement of reliability, the possibility of residual flit error rate is measured in terms of probability of Decipher fails to point-out errors. The above factor quantifies the reliability of different error control methods. The possibility of the proposed QMEC scheme is calculated initially with the help of probability of exact decoding. The general rule of probability implies over here as the sum of the probability of residual and probability of correct decoding equals unity which shall also be depicted as [19] in eqn. 5.

$$P_{resid} = 1 - P_{crt} \quad (5)$$

The proposed QMEC is rectifying nonuple random errors or conjunction of both random and burst errors totaling nonuple. The following two noise scenarios are considered to calculate the residual flit error rate for the proposed QMEC,

a. Exclusively random errors, where P_c=0
b. Conjunction of random and burst errors where P_c=10^{-2}

2) Exclusively random errors where P_c=0

When, P_c = 0the desired possibility is the random error which results in zero coupling probability. Due to the above, the noise heads that affects the adjoining wire tickles to zero resulting in occurrence of random errors only. In order to know the residual flit rate of the above, it is important to calculate the possibility of the exact decoding for random error. The projected QMEC coding schemes encodes 'm' message bits as (5m, m).

As a result, it is possible for the proposed QMEC code to correct more flits than this and the probability is calculated by taking all the possibilities of correct decoding into account. Thus, the probability is mentioned as below eqn. 6 [19],

$$P_t(crt,rnd) \geq P_t(5m,1) + P_t(5m,2) + P_t(5m,3) + P_t(5m,4) + P_t(5m,5) + P_t(5m,6) + P_t(5m,7) + P_t(5m,8) + P_t(5m,9) \quad (6)$$

Pt(5m,1), Pt(5m,2), Pt(5m,3), Pt(5m,4), Pt(5m,5), Pt(5m,6), Pt(5m,7), Pt(5m,8), Pt(5m,9) are the probabilities of errors with zero, one, two, three , four, five, six, seven , eight and nonuple in a (5m) number of bits. With BER (τ), eqn. 7 provides the probability of 't' errors in 'm' number of bits [19].

$$P_t(m,t) = \binom{m}{t} \tau^t (1-\tau)^{(m-t)} \quad (7)$$

The below eqn. 8 represents $P_{crt,rnd}$, for the proposed QMEC scheme.

$$P_{crt,rnd} = \sum_{t=0}^{9} \binom{5m}{t} \tau^t (1-\tau)^{(5m-t)} \quad (8)$$

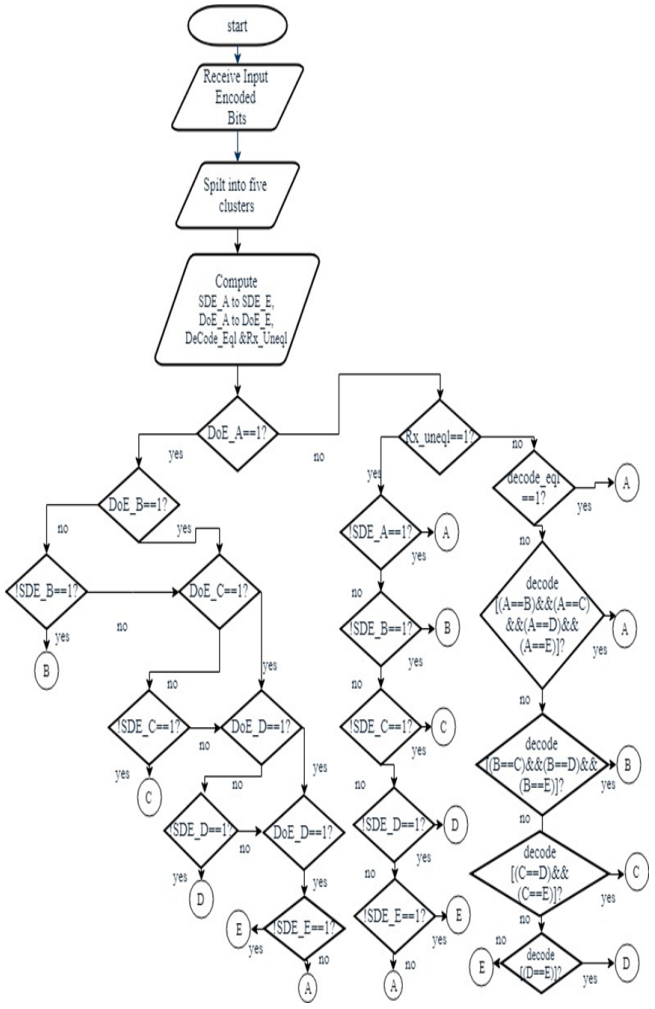

Figure 3. Flow Graph of the proposed QMEC Decipher's nonuple algorithm

The residual flit error's probability P_{resid} is given as expressed in eqn. 9 by substituting eqn. 8 in eqn. 5.

$$P_{resid} = \binom{5m}{10}\tau^{10} \tag{9}$$

3) Conjunction of Multiple Random Errors and Burst Error

Let us consider Pc= 10^{-2}, which ensures the occurrence of a conjunction of multiple random errors and burst error. As the coupling probability Pc is not zero, the adjacent wire is much affected by noise sources and leads to the probability of burst error too. Let us consider the three burst errors and six random errors. Eqn. 10 gives the probability of the residual flit error [19].

$$P_{resid} = 1-(P_{crt,rnd} + P_{crt,burst}) \tag{10}$$

P_{resid} is obtained by incorporating eqn.4 and eqn.7 in eqn. 10 and is given as eqn. 11

$$P_{resid} = 1-\sum_{t=0}^{5}\binom{5m}{t}\tau^{t}(1-\tau)^{(5m-t)} + P_c^{\,2}\tau \tag{11}$$

D. Link Swing Voltage

Energy and voltage are proportional to each other as the increase in energy consumption consumes more voltage. However, the most important aspect is when the error coding schemes are applied it increases the reliability at the expense of a decrease in the link-swing voltage and energy. The Inclusion of error control method improves the reliability level, which reduces the swing voltage as they can accept more noise boundaries. As the noise margins are tolerated, it literally saves the power as the link depends quadratically on swing voltage as expressed in eqn.12. The power consumption relays on the error controlling schemes and thereby uses low voltage. The following equation relates the swing voltage to the reliability [19],

$$V_{sw} = 2\sigma n Q^{-1}(\xi) \tag{12}$$

Where Q-1(ε) is the inverse Q function and (ε) is the value at which P_{resid} (ε) = P_{req} where P_{req} is the required flit error rate.

E. Link Power Consumption

Capacitance C, the link-switching factor β, the wire width W_w, the swing link voltage V_{sw}, and the clock frequency fc comprises the link power consumption PW_w. It is the product of the above and expressed as eqn. 13 [19, 33].

$$PW_w = C.\beta.W_w.V_{sw}^{\,2}.f_c \tag{13}$$

Where β is is 0.5 and the error control schemes decide the W_w. According to eqn. 12 requirements of various error control method reliability determines the link swing voltage V_{sw}. The Low error correction capable error control scheme requires more link swing voltage than error control technique with more error correction capability [19].

IV. Analysis of the Performance of Proposed QMEC Codec

Area, power consumption and delay of Codec, residual flit error rate, interlink power and link-swing voltage and reliability are the prime factors that account for the performance of the proposed QMEC compared to other codes considered for the experimental purpose are discussed in this chapter. A 32-bit flit is used for the performance analysis. The proposed QMEC is compared with Ex-Hamming Code, DAP, CADEC, JTEC [18], MBRBEC codec [19], Manchester based MBRBEC, Proposed QMEC codec without Manchester and proposed QMEC codec.

A. Analysis of the Codec Power, Area and Delay

The performance of the proposed QMEC codec along with other error correcting codes is evaluated by implementing the schemes in Vivado 15.1 for the Zynq7000 series xc7z020clg484-1chip. The relationship between power consumption, FPGA resource utilization and delay were compared for the schemes. The evaluation was carried out using 32-bit flit in the device mentioned above. Table I shows the power consumption, area utilization and delay by different codecs ran through it.

As depicted in the above Table I, it is evident that each codec has error correcting capability ranging from single to a maximum of five bits in the earlier researches; however, our proposed technique, QMEC has error correcting capability of nine bits. This is a significant improvement over state-of-the-art techniques. Each bit is coded and decoded with respective error controlling codec in the tool. MBRBEC code [19], which corrects up to five errors, has edged out the area and power consumption by 6% and 63% when Manchester scheme is incorporated into it. This depicts the impact of Manchester coding that plays a crucial role in the power.

It is evident that the increase in the power is directly

proportional to the utilization of area, which also empowers the number of error corrected. Area and power consumption decreases with the incorporation of Manchester encoding emphasizes DC component of the data. The proposed QMEC codec corrects nonuple errors with cross talk avoidance by the process of quintuplication. The proposed QMEC codec without Manchester consumes more power and LUTs, which is 57% and 35% than MBRBEC. As QMEC without Manchester corrects the nine-bit error, the power consumption per corrected error bit is 2.2 than MBRBEC, which is 2.6. It is more prominent that when Manchester code is included in QMEC, reduces the power by 16% and reduces the number of LUTs by 1% compared to MBRBEC. When Manchester coding is embedded with MBRBEC and QMEC, the power consumption per number of error correction bits reduced to 1.6 and 1.78 respectively.

The delay in MBBREC with Manchester is almost equal to JTEC but significantly lesser of MBBREC. Also, the delay of the proposed QMEC is less than QMEC without Manchester. The reduction in power, area and delay is because of half the size of the data transition through Manchester coding.

B. Residual Flit Error Rate

The residual error rates of different error coding schemes are depicted in Fig. 4a and Fig. 4b with noise voltage deviation. In order to better understand the residual error rate, two of the noise situations of different techniques such as (a) Only nonuple random errors (b) mix of six random and three burst errors are considered. For better understanding, we use Pc= 10^{-2} and Pc = 1 as coupling probability in the simulations. 1.0V serves as the inter link-swing voltage and the simulation results of residual flit error rate of random errors with various error control are depicted in Fig. 4a. Though we ran eight different scenarios, considered only DAP, CADEC, JTEC, MBRBEC and proposed QMEC for computing the results. Compared to the results of other error correcting codes, the proposed QMEC code corrects both random errors and conjunction of random and burst errors by recording much order of low residual flit error rate than other error control codes [19,20]. QMEC code is unique as it can correct nonuple errors, which is significantly high when compared to other code schemes represented here.

CADEC and JTEC have performed well as they both correct errors up to two and three respectively. In Fig. 4b, the residual flit error rate of the conjunction of multiple random and burst errors determined by the noise voltage deviation. QMEC code registered a low residual rate in correcting the combination of errors and proved that the proposed code is capable of correcting errors extending to nonuple. The graph also picturizes the residual rate of DAP (65, 32) flit which raises as result of a failure of correcting burst error [19] while the CADEC and JTEC have low residual flit error rate compared to DAP as they can correct errors of two and three only. MBRBEC code had a better edge in correcting the errors accounting to five when compared to others as it has slightly higher error correcting capability but the QMEC code uses a unique system where the data size reduced to half of it before passing through the Decipher and corrects nonuple errors.

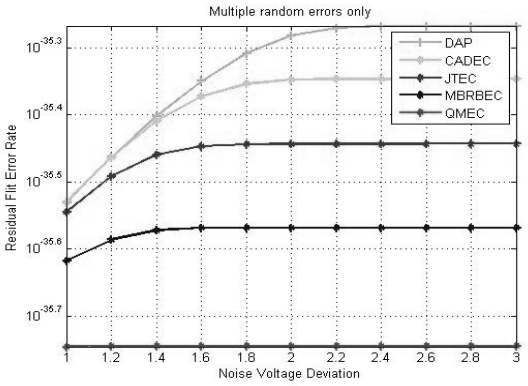

Figure 4a. Multiple random errors only

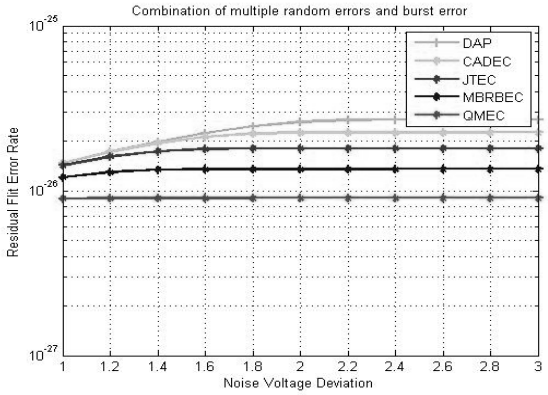

Figure 4b. Multiple random errors and burst errors combined

C. Voltage consumption Evaluation

The performance of low swing voltage by different error controlling codes is explained in Fig. 5. The proposed QMEC code achieves 71% reduction in voltage consumption the d flit error rate of 10-20 than MBRBEC and corrects nonuple errors in contrast to five by MBRBEC. The implementation of MBRBEC reduces the Voltage by 61% than DAP. The swing voltage in QMEC reduced to 91% and 97% compared to DAP and CADEC respectively. QMEC has edged out the MBRBEC significantly by 30% in DAP. A reduction of 95% in voltage consumption compared to JTEC indicates that the QMEC code has a significant impact when incorporated with Manchester coding. The proposed QMEC consumes low link-swing voltage compared to other methods of error controlling.

D. Link Power Consumption Analysis

The codec link-power consumption of various techniques of error control is shown in Fig. 6. In our earlier results, it has been mentioned that the proposed QMEC has high reliability while consumes less voltage which is proportional to link power consumption with link length of 1mm. For the given the scenario with 10^{-20} reliability requirement, the power consumed by the link is noted for various error-controlling schemes of DAP, CADEC, JTEC, MBRBEC and proposed QMEC. The DAP and CADEC consumed same power while the former Corrected only one

TABLE I. ANALYSIS OF VARIOUS ERROR CONTROL SCHEMES

Name of the Codec	Crosstalk avoidance	Error Correction (No. of Bits)	No. of LUTs	Ratio= No. of LUTs/No. of bits	Power (mW)	Ratio = Power/ No. of bits	Delay (ns)
Ex-Hamming Codec	No	Single	19	19	1.04	1.04	0.027
DAP	Duplication	Single	4	4	0.74	0.74	0.015
CADEC	Duplication	Double	115	57.5	9.2	4.6	0.178
JTEC	Duplication	Three	117	39	11.7	3.9	0.267
MBRBEC	Triplication	Five	121	24.2	13	2.6	0.35
MBRBEC with Manchester	Triplication	Five	114	22.8	8	1.6	0.28
Proposed QMEC without Manchester	Quintuplication	Nonuple	279	31	20	2.2	1.09
Proposed QMEC	Quintuplication	Nonuple	276	30.67	16	1.78	0.89

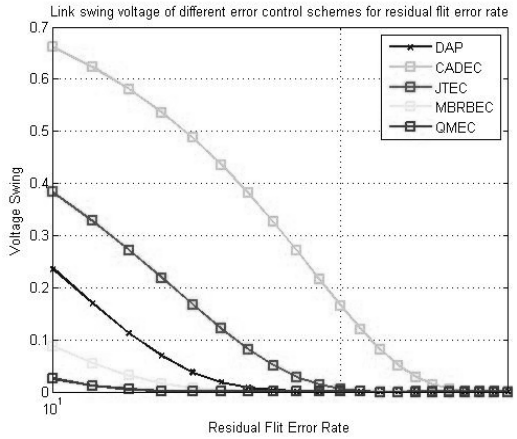

Figure 5. Analysis of Link Swing Voltage

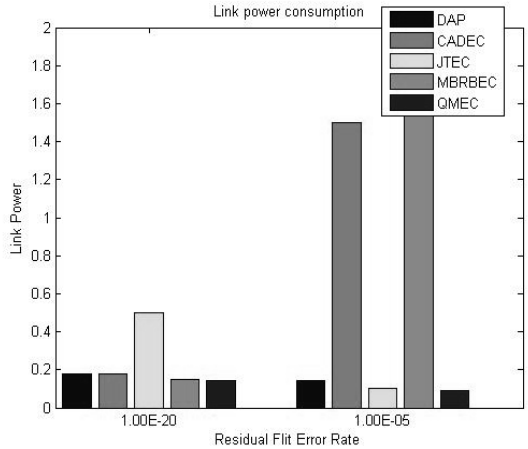

Figure 6. Link power consumption of different error control schemes for 1mm link length

residual error and the latter corrected two. JTEC rectifies three errors with a phenomenal usage of power while the MBRBEC corrects five errors consuming power much lesser than JTEC. The link power consumption of QMEC is 11 % less than DAP and CADEC while 66% than JTEC. It has shown a reduction of 6% than MBRBEC, which is significant. The case is similar for 10^{-5} with the proposed QMEC consumes 53% less than DAP, while it achieved 20% less than JTEC. QMEC consumed 84% and 85% less link power than CADEC and MBRBEC respectively. The implementation of Manchester coding in QMEC was effective in correcting nonuple errors and consumes less power than MBRBEC, which is evident with the results depicted above.

V. CONCLUSION

In this paper, the performance of the proposed QMEC code has been studied and compared with DAP, Ex-Hamming Code, CADEC, JTEC, MBRBEC. The QMEC corrects nonuple errors than five errors by MBRBEC of any scenario of exclusively random errors or multiple random and burst errors with crosstalk avoidance. This is a significant improvement over state-of-the-art techniques, which can correct only up to a maximum of five-bit errors, representing an improvement of 80%.

The proposed QMEC though utilizes more LUTs but consumes 16% less power when compared to MBRBEC. QMEC effectively dissipates the voltage irrespective of the increase in LUTs while consuming 85% low link power than MBRBEC. To study the error correcting capability, the residual flit error of all the above-mentioned codes were compared with QMEC, which outlines other codes with low residual flit error rate and low swing voltage up to 95% Hence, QMEC significantly provided high reliability by correcting nonuple errors with little increase in area and less link power consumption.

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