Design Options for Current Limit and Power Limit Circuit Protections for LDOs

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***Abstract*—This paper presents novel circuitry for protection of the power transistor in LDOs with adjustable output voltage implemented in BJT technologies. First, an improvement is proposed to a current limit circuit reported previously, that significantly reduces the variation of the value the output current is limited to, caused by setting the output voltage to different values. Next, two circuits for ensuring that the power transistor operates within its safe operating area are introduced; they are based on the proposed current limit circuit, but its activation point is no longer proportional to the output current but to the sum of the output current and a current proportional to the voltage drop across the power transistor. Finally, a circuit that monitors and limits the power dissipated is described; it also employs the proposed current limit circuit but this time the activation point is proportional to the product of the output current and the voltage drop across the power transistor. Three LDOs that employ the three types of protections proposed here are then compared, considering the power dissipated by the power transistor and the resulting maximum die temperature.**

***Index Terms*—current limiters, power dissipation, power system protection, short-circuit currents, thermal analysis.**

I. INTRODUCTION

A low drop-out voltage regulator (LDO) dissipates surplus power as heat and this could cause excessive temperature rise on the power stage, T_{PASS}. To prevent destructive effects the die temperature should be maintained bellow a safe threshold [1] by limiting the product of the output current by the voltage drop across the pass transistor ($P_{Tpass}=V_{DROP}*I_Q$, where $V_{DROP}=VIN-VQ$).

Short-circuits or overload situations are typical fault conditions for electronic devices [2-3]. In these scenarios the accuracy of the protection circuits is essential for the reliability and the robustness of the LDOs [4-5]. The simplest protection circuit to maintain the power dissipated bellow a set maximum value is the current limit protection [6-11]. The current limit circuitry sets the maximum value the output current can take, called here I_{Qlimit}, thus indirectly confining the maximum power dissipated by T_{PASS}. A typical current limit implementation is shown in Fig. 1: a fraction of the output current I_Q is sourced into a resistor and the resulting voltage is compared against a voltage reference; in Fig. 1 these voltages are denoted V_{SENSE} and V_{REF}, respectively. When V_{SENSE} gets larger than V_{REF} the current limit circuit is activated, that is, the NPN transistor driven by the comparator turns off, sinking the current I_{CLOUT} from the Error Amplifier (EA); thus, the main feedback loop implemented by the EA is broken. Instead, a new negative feedback loop is established by the current limit circuit and transistors T_{DRIVER}, T_{PASS} and T_{SENSE} that ensures the equality between V_{SENSE} and V_{REF} by controlling the output current – effectively setting its value to I_{Qlimit}.

When the output is shorted to ground the V_{DROP} reaches its worst-case (maximum) value leading also to the maximum value of the P_{Tpass}. Important temperature gradients can appear across the power stage, leading to hotspots (locations where the die temperature peaks) which could increase even more the I_{Qlimit}. If the current limit circuit has a large and positive temperature coefficient this could result in increasing the I_{Qlimit} value, thus larger P_{Tpass} and increasingly larger die temperature and the eventual chip destruction.

The fold-back current limit approach is a better choice for a large input voltage domain since this type of protection, once activated, reduces the values of both the output voltage (VQ) and current, I_{Qlimit}, therefore reducing P_{Tpass}. However, the fold-back current limiting has to deal with latch-up issues after an overload condition [12-14].

Another important aspect is the I_{Qlimit} variation with temperature; the standard solution is to implement a complementary to absolute temperature (CTAT) characteristic for I_{Qlimit}, as shown in Fig. 2 [14]. But this results in a larger power being dissipated at lower temperatures and a possible destruction mechanism of the device [15]. One potential solution is to implement an architecture that employs a temperature calibrated current limit protection as presented in [16]. But this approach results in complex structures that require large die area and quiescent current. Even so, this will not guarantee the robustness of the IC if the inherently un-even temperature distribution across the LDO is not taken into consideration and hot-spots are not controlled.

For a robust design one must ensure that all devices, T_{PASS} in particular, stay within their safe operating area (SOA) for all operating scenarios, including predictable improper usage [17]. The SOA of a power device is outlined by three electrical parameters: current, voltage and power [16]. Therefore, limiting the current is not always sufficient to avoid the destruction region; in some cases, it is also necessary to control the dissipated power of the IC. For an LDO the factor V_{DROP} is largely outside designer's control but it can be monitored and the I_{Qlimit} can be dynamically optimized accordingly to limit the power dissipated.

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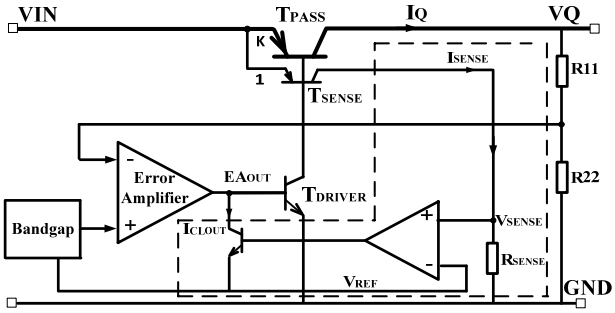

Figure 1. Typical Implementation of a current limit protection for an LDO with PNP pass transistor

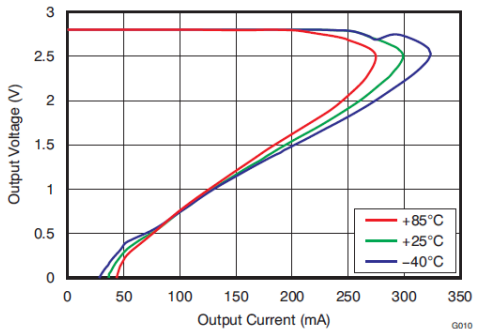

Figure 2. Temperature variation of the output current for an LDO with foldback current limit protection ([14])

The paper is organized as follows: Section II starts with a brief analysis of the low-power current limit implementation reported in [19]; next, an improved solution is presented, that significantly reduces the variation of the value the output current is limited to, caused by setting the output voltage to different values. Section III present two circuit solutions for ensuring that T_{PASS} operates within its SOA; they are based on the current limit circuit proposed in Section II, but its activation point is made proportional to the sum of I_Q and a current proportional to the voltage V_{DROP}. A novel power limit circuitry for LDOs is presented in Section IV; it also employs the proposed current limit circuit but this time the activation point is proportional to the product of I_Q and V_{DROP}. Three LDOs that employ the three types of protections discussed here are compared in Section V. Section VI presents a summary and the main conclusions drawn from this work.

II. Current Limit Circuitry

A. Analysis of existing solutions

Most of the published current limit architectures occupy large die area and consume fairly large quiescent current [6-13]. The current limit circuitry proposed in [19] (shown in Fig. 3) overcomes these drawbacks: the circuitry is biased only by the sensed branch (I_{SENSE}) and the area occupied is quite small. For the circuit shown in Fig. 13 the current limit circuit takes in I_{SENSE} and the trip point value, I_{CLtrip}, is temperature independent:

$$I_{CL} = I_{SENSE} \Rightarrow I_{CL_{TRIP}} = \left[\left(\frac{V_T \ln m}{R_3} + \frac{V_{BE3}}{R_4}\right) \cdot \frac{R_2 + R_1}{R_1}\right] \quad (1)$$

The I_{Qlimit} is obtained by multiplying the trip point, I_{CLtrip}, with the current gain of T_{PASS}-T_{SENSE} mirror, considering not only the ratio k between these transistors but also the fact that their collector-emitter voltages are quite different:

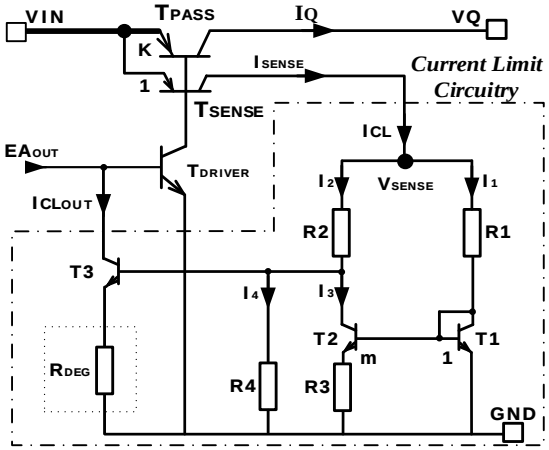

Figure 3. Schematic of the current limit circuit proposed in [19]

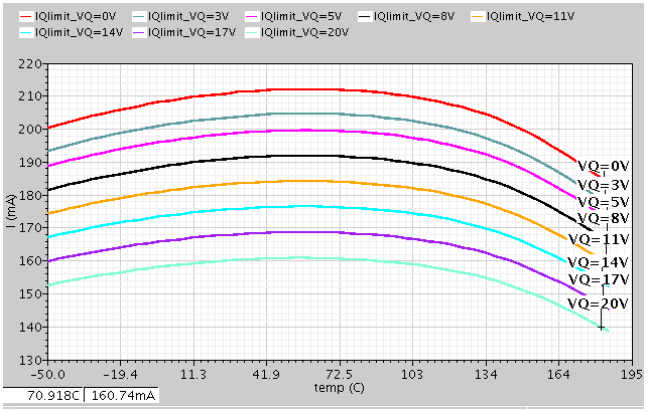

Figure 4. Variation with temperature and output voltage (values between 0V and 20V) of the I_{Qlimit} for the circuitry shown in Fig. 3 [19]

$$I_{Qlimit} = k \cdot I_{CL_{TRIP}} \cdot \frac{1 + \frac{VIN - VQ}{V_A}}{1 + \frac{VIN - V_{SENSE}}{V_A}} \quad (2)$$

where V_A is the Early voltage of T_{PASS} and T_{SENSE}.

Fig. 4 details the simulated temperature variation of the I_{Qlimit} for different VQ values. The relative variation with temperature is below 15% for the wide temperature range of -50°C to 185°C (the automotive temperature domain plus the range until the thermal shutdown protection is activated). However, the variation of the I_{Qlimit} value due to VQ taking values between 0V and 20V is far larger: about 60mA. The root cause of this variation is the fact that transistors T_{PASS} and T_{SENSE} have different emitter-collector voltages – see (2): VQ can be programmed to different values (or go down to zero in shorted-output conditions) but V_{SENSE} has approximately the same value.

Obviously, the current limit protection should not interfere with the normal operation; it follows that for this circuit the maximum output current in normal operation should be kept well below 140mA, although the circuit itself could withstand at least I_{Qmax}=215mA. Moreover, for VQ =0 both the V_{DROP} and the I_{Qlimit} take their maximum values, resulting in a sharp, potentially dangerous increase of the power dissipated by the T_{PASS} transistor.

B. Proposed solution and simulations results

Fig. 5 presents an improved version of the circuit shown in Fig. 3, which significantly reduces the I_{Qlimit} dependency on the output voltage VQ, by forcing V_{SENSE} to follow VQ:

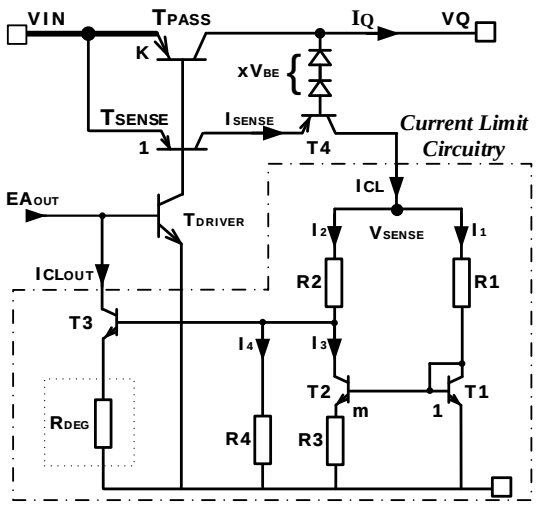

Figure 5. Schematic of the improved current-limit circuit

$$V_{SENSE} = VQ + x \cdot V_{BE} \quad (3)$$

Two facts should be considered when setting the value of *x:* i). V_{SENSE} should be large enough for the circuit to operate over the entire VQ range, particularly for VQ=0 (output shorted to ground); ii). The current limit circuitry will not perform its function when V_{DROP} gets smaller than xV_{BE}. The later is a useful feature rather than a shortcoming: for small V_{DROP} values the power dissipated by T_{PASS} transistor remains small, even if the output current gets over the I_{Qlimit} – see the current peak in the first part of Fig. 6.

Fig. 7 is the counterpart of Fig. 4: it presents on the same scale and under same conditions the variation with temperature and VQ of the I_{Qlimit} value for the circuit shown in Fig. 5. Direct comparison between Fig. 7 and Fig. 4 demonstrates the significant improvement provided by the circuit proposed in Fig. 5: the maximum I_{Qlimit} variation due to VQ taking values between 0V and 20V is now below 2mA, over 30 times smaller than the variation shown in Fig. 4 for the same conditions. Moreover, the absolute maximum value of the output current is down from 215mA to 167mA. Thus, the designer has two options for increasing the performances/cost ratio of this circuit in comparison with the one shown in Fig. 4: the maximum load current can be increased by roughly 50mA by simply setting the I_{Qlimit} to a larger value or, if the requirements for the maximum load current and I_{Qlimit} value remain the same, the size of transistor T_{PASS} can be reduced by approximately 25%. Monte Carlo simulation results presented in Fig. 8 provide further information for these options.

Figs. 6-8 and Fig. 9 (top) show that I_{Qlimit} vary relatively little with temperature and VQ and it is fairly independent on process variations; also, it does not vary significantly with the input voltage, once V_{DROP} gets large enough. But the power dissipated by T_{PASS} remains proportional to the drop-out voltage, as shown in Figure 9 - bottom.

III. Circuitry for SOA Protection

A. *Brief analysis of a popular solution*

To ensure that transistor T_{PASS} remains within its SOA one should control the power dissipated by it. For this the current-limit circuits should be modified so that the effective I_{Qlimit} value decreases as the drop-out voltage increases. A typical implementation of such a SOA protection circuitry is

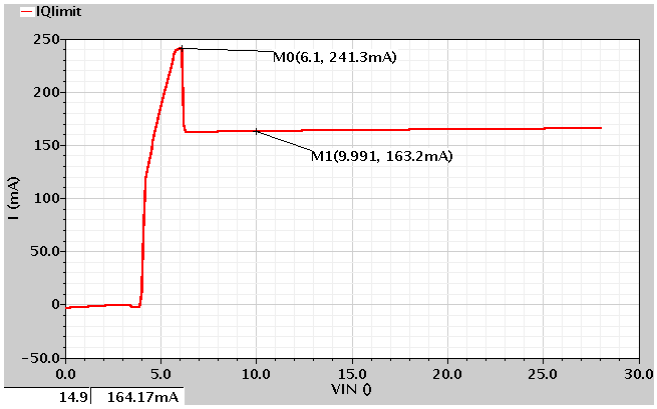

Figure 6. Variation of the output current provided by the circuit shown in Fig. 5 when the input voltage is increased steadily from 0V to 28V. The output voltage was set to 5V and the temperature was kept constant at 25°C

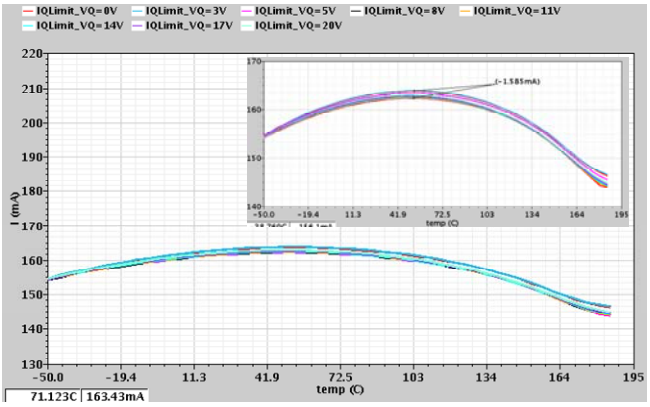

Figure 7. Variation of the I_{Qlimit} value with temperature for the improved current-limit circuit, when the output voltage is set to values between 0V and 20V. The zoom-in view shows that the max-min variation is 1.585mA.

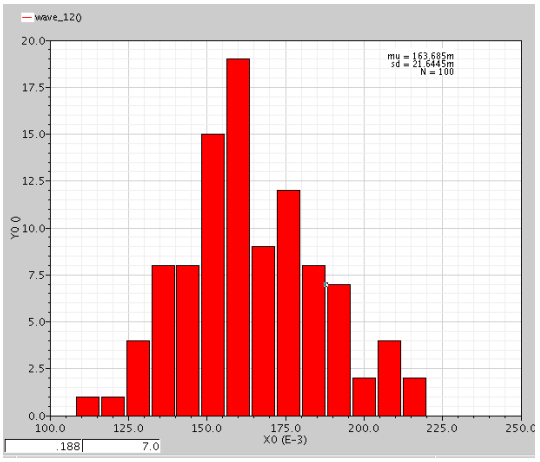

Figure 8. Monte Carlo simulations for I_{Qlimit} value of the circuit shown in Fig. 5 when VQ is set to 5V and the temperature is kept constant (25°C)

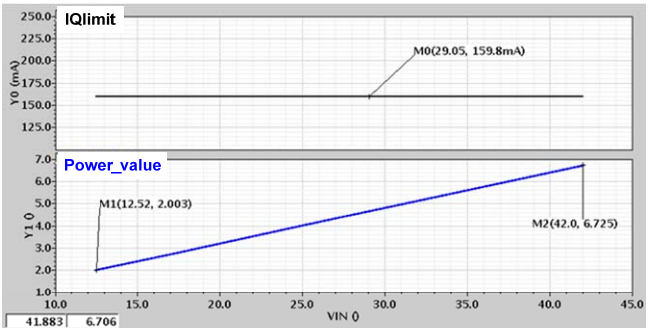

Figure 9. Variation of the I_{Qlimit} value (top) and the power dissipated by T_{PASS} (bottom) for the circuit shown in Fig. 5 when the input voltage is increased steadily from 12.5V to 42V. The output voltage was set to 5V and the temperature was kept constant at 25°C

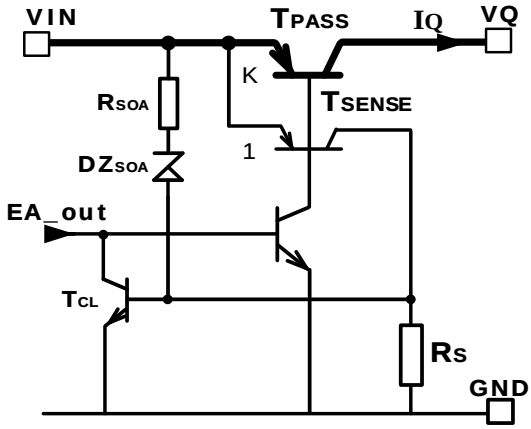

Figure 10. The current-limit circuit with SOA protection proposed in [20]

presented in Fig. 10, [20]. The additional SOA circuitry consists of R_{SOA} and DZ_{SOA}: when the input voltage, VIN, reaches a certain threshold ($V_{TH}=V_{BECL}+V_{DZSOA}$) an additional current (beside the sensed current) is sourced into R_S, thus reducing the effective I_{Qlimit} value by an amount proportional to (VIN-V_{TH}), which approximates V_{DROP}. This approach works fairly well when VQ has a fixed value, but it is not suited to LDOs with adjustable output voltage.

B. Proposed SOA protection based on current limit circuits with I_{Qlimit} value inversely proportional to V_{DROP}

The current limit circuitry proposed in Section II.B can be adapted to control the power dissipated by T_{PASS} by making the value of I_{Qlimit} inversely proportional to V_{DROP}. Two design options for V_{DROP} sensing are presented in Figs. 11-12. A comparative analysis is performed on the two circuits, to highlight their relative advantages and limitations, focusing on their quiescent current and die area.

The trip point of the current limit circuitry is expressed by (1) but an offset current (I_{DROP}), which is proportional with the drop-out voltage, V_{DROP}=VIN-VQ, is added to I_{SENSE}. I_{DROP} for the circuit shown in Fig. 11 has the expression:

$$I_{DROP} = I_{IN} - I_Q = \frac{VIN - V_{BE10}}{R} - \frac{VQ - V_{BE13}}{R} = \frac{VIN - VQ}{R} \quad (4)$$

Where the base-emitter voltages of transistors T_{10} and T_{13} are considered equal. In this case the I_{Qlimit} expression is:

$$I_{Qlimit} \simeq k \cdot I_{CL_{TRIP}} = k \cdot (I_{SENSE} + I_{DROP})_{TRIP} \quad (5)$$

The expression of I_{DROP} is the same for the second design option for V_{DROP} sensing, shown in Fig. 12. There, I_{DROP} is obtained across the resistor R by applying at its terminals buffered versions of the input and output voltages. This current can be used as an offset current for the trip point of the current limit circuit, effectively modifying the I_{Qlimit} value according to V_{DROP}.

Both structures presented in Figs. 11-12 realise currents proportional to V_{DROP} but their quiescent currents are quite different: the quiescent current of the first design option (Fig. 11) depends on both the input and output voltages while the second design option (Fig. 12) requires a constant quiescent bias. But the circuit shown in Fig. 12 occupies a far larger area than the one shown in Fig. 11.

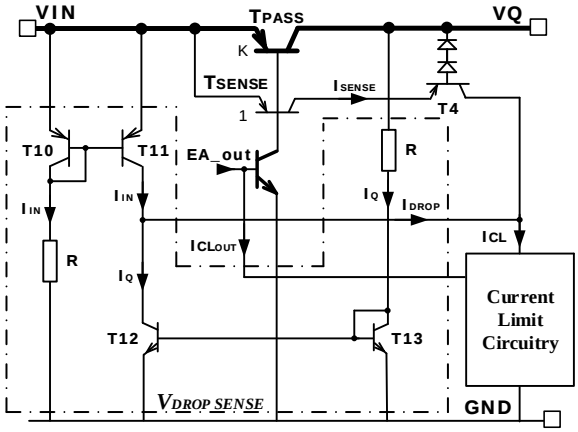

Figure 11. SOA protection based on the current-limit circuit shown in Fig. 5 and the first design option for implementing the necessary V_{DROP} sensing

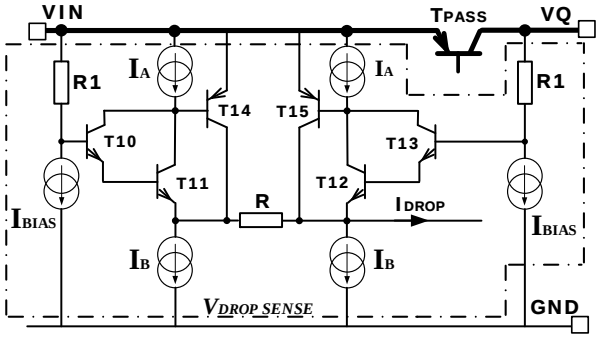

Figure 12. Second design option for implementing V_{DROP} sensing for the SOA protection

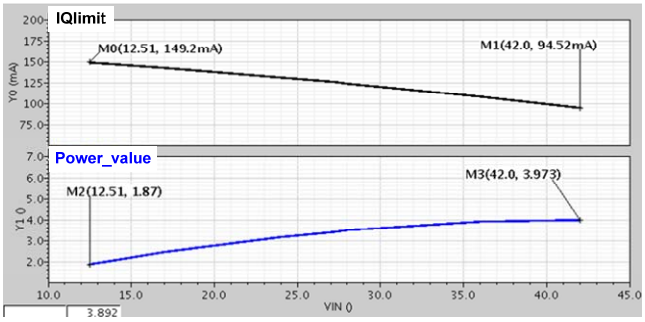

Figure 13. Variation of the I_{Qlimit} value (top) and the P_{Tpass} for the circuit shown in Fig. 9 when the input voltage varies between 12.5V to 42V

Fig. 13 presents the variation with the input voltage of the I_{Qlimit} value and the power dissipated by T_{PASS} for the circuit shown in Fig. 11; a very similar set of plots were obtained for the circuit shown in Fig. 12. Fig. 13 is a direct counterpart of Fig. 9, so by comparing these two figures one can assess the advantages of the circuits presented in this section (shown in Figs. 11 and 12) over the circuit shown in Fig. 5. The main ones are the smaller maximum value of dissipated power and the smaller ratio between the maximum and minimum values of the dissipated power: (N=3.973W/1.87W) compared to (N=6.725W/2W) for the circuit in Fig. 5. The small nonlinearity of the I_{Qlimit}=f(VIN) characteristic is caused by transistors T_{10} and T_{11} operating at different emitter-collector voltages.

IV. Protection Based on Power Limit Circuits

T_{PASS} consists of numerous transistors connected in parallel that operate at different temperatures due to the non-uniform temperature distribution within the die. Over-temperature protection – not discussed here - may not be

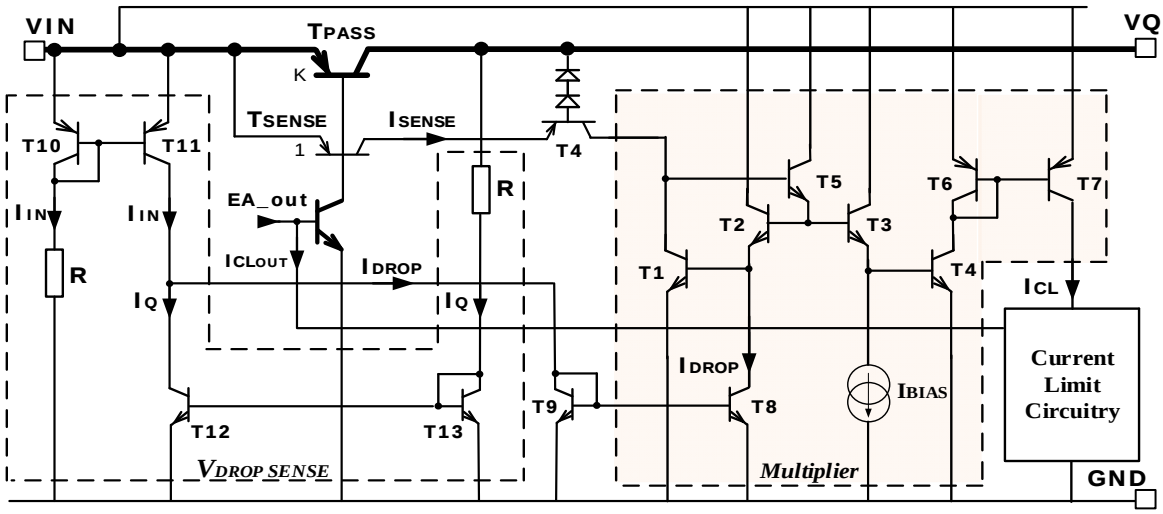

Figure 14. Proposed circuit for power limit protection of LDOS

effective if the difference between the sensed temperature and the hot-spots (zones with largest die temperature) is not known. The approach here is to prevent the apparition of hot-spots by monitoring the power dissipated by T_{PASS} and dynamically adjusting the I_{Qlimit} value of a current-limit circuit based on the ones shown in Figs. 5 and 11.

The proposed circuit is presented in Fig. 14. The dissipated power is derived by multiplying the current I_{DROP}, proportional to V_{DROP} – see Fig. 11 and (4), with the current I_{SENSE}, proportional to the load current – see Fig. 5. The multiplier is implemented by transistors T1-T7 [21-22]. Its output current is used as input for the current limit circuitry (I_{CL}); the I_{Qlimit} expression results as follows:

$$V_{BE2} + V_{BE1} = V_{BE3} + V_{BE4} \tag{6}$$

$$V_T\left(\ln\frac{I_{SENSE}}{I_S} + \ln\frac{I_{DROP}}{I_S}\right) = V_T\left(\ln\frac{I_{BIAS}}{I_S} + \ln\frac{I_{CL}}{I_S}\right) \tag{7}$$

$$I_{CL} = \frac{I_{SENSE}\cdot I_{DROP}}{I_{BIAS}} \tag{8}$$

$$I_{Qlimit} \simeq k\cdot I_{CL_{TRIP}} = k\cdot\left(\frac{I_{SENSE}\cdot I_{DROP}}{I_{BIAS}}\right)_{TRIP} \tag{9}$$

where I_S is the saturation current (transistors T1-T7 have the same area) and I_{BIAS} is a constant current.

Obviously, I_{Qlimit} is proportional to the dissipated power, $P_{Tpass}=V_{DROP}*I_Q$; it follows that the current-limit loop will also control P_{Tpass}. Fig. 15 is the counterpart of Figs. 9 and 13, obtained for an LDO that employs the circuit shown in Fig. 14. It proves that the dissipated power is fairly independent on the input voltage, thus on V_{DROP}, as well.

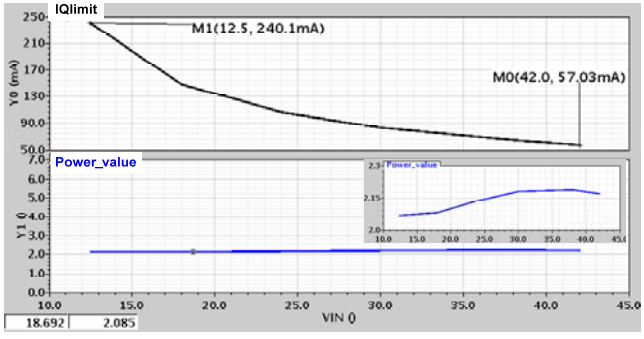

Figure 15. Variation of the I_{Qlimit} (top) and the P_{Tpass} (bottom) for the circuit shown in Fig. 14 when the input voltage varies between 12.5V to 42V

V. Comparison of Protection Circuits Shown Here

A comparison of the protection circuits presented in this paper is detailed in Table 1. For a fair comparison the simulations are performed in the same scenario: the overload condition is triggered by externally forcing the output voltage at 90% of its nominal value (VQ constant) while the input voltage is varied from 12.5V up to 42V; the I_{Qlimit} and the P_{Tpass} are monitored and their minimum and maximum values are extracted. For all these simulations the temperature is kept constant at 25°C.

It is noticeable that the ratio between the maximum and the minimum power dissipated (N) its almost 1 for the LDO with power limit protection (constant power) but for this protection type I_{Qlimit} has the largest variation. Instead for the LDO with current limit protection only, N has the highest value (N=3.35) although the I_{Qlimit} is constant.

The maximum P_{Tpass} for all protection types occurs when the input voltage reaches his maximum value (V_{IN}=42V – see Figs. 5, 11 and 14). For this scenario we performed thermal simulations using the simulator presented in [23]. The starting temperature was set to 150°C in each case and the power applied is established according to Table 1. The thermal simulations also consider the layout of the LDOs and the physical description of the package.

The results are shown in Fig. 16 and suggest that the LDO with power limit protection has the flattest temperature distribution while the maximum temperature (hotspot) is below 190°C. This indicates that by using the power limit protection one may no longer need the over-temperature protection for LDO. By contrast the LDO with current limit protection only has an uneven temperature distribution map and the hotspots can reach 250°C.

Table I. Comparison of the Protection Types used for LDOs Regarding the I_{Qlimit} and the P_{Tpass} Values

Protection Type	I_{Qlimit} MAX [mA]	I_{Qlimit} MIN [mA]	P_{Tpass} MAX [W]	P_{Tpass} MIN [W]	N= $P_{TpassMAX}$ /$P_{TpassMIN}$
Current Limit (Fig. 5)	159.8	159.8	6.725	2.003	3.35
Current Limit with Circuitry for SOA (Fig. 11)	149.2	94.52	3.973	1.87	2.12
Power Limit (Fig. 14)	240.1	57.03	2.18	2.07	1.053

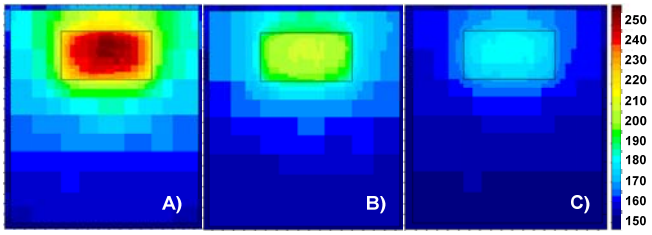

Figure 16. Temperature maps for the protection types presented – Current limit only (A), current limit with circuitry for SOA protection (B) and power limit protection (C)

VI. Summary and Conclusion

This paper presents novel circuitry for protection of the power transistors (T_{PASS}) in LDOs with adjustable output voltage. For this type of LDOs the output voltage can be set to different values - in our case VQ can take values between 0V and 20V. This characteristic can increase the variation of the value I_Q is limited to. First, an improvement is proposed for a state-of-the-art current limit protection which reduces the output voltage variation of the I_{Qlimit} by a factor of 44 (from 65mA to 1.5mA) using approximately the same area and no additional quiescent current. Moreover, keeps the advantages of the previous circuitry: the I_{Qlimit} vary relatively little with temperature and it is fairly independent on process variations. Based on this development two options for increasing the performances/cost ratio are detailed: the I_{Qmax} can be increased by roughly 50% by simply setting the I_{Qlimit} to a larger value or, if the requirements for the I_{Qmax} and I_{Qlimit} value remain the same, the size of T_{PASS} can be reduced by approximately 25%.

Another particularity of adjustable LDOs is that for the same VIN the voltage drop across T_{PASS} (V_{DROP}) could vary in a large domain. To ensure that T_{PASS} operates within its SOA in all scenarios it is necessary to monitor the V_{DROP} and adjust the I_{Qlimit} accordingly. Regarding this, two design options for V_{DROP} sensing were proposed; they are based on the previously suggested current limit circuit, but its activation point is no longer proportional to the I_Q but to the sum of I_Q and a current proportional to V_{DROP}. The advantages of these architectures consist in the smaller maximum value of P_{Tpass} and a smaller ratio between the maximum and minimum values of the dissipated power: N=2.12 compared to N=3.36 for the current limit protection only circuit.

Finally, a circuit that monitors and limits the P_{Tpass} is described; it also employs the proposed current limit circuit but this time the I_{Qlimit} is dynamically adjusted based on the P_{Tpass} value. Three LDOs that employ the three types of protections proposed here are implemented and then compared, considering the P_{Tpass}, and the resulting maximum die temperature, when the output voltage is kept constant at 90% of its nominal value while the input voltage is varied over a wide range. Electrical and thermal simulations showed that for the LDO with power limit protection the P_{Tpass} is almost constant (N=1.053) for a large VIN domain and the temperature distribution is the flattest compared to the other proposed protection types.

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