Analysis and Control of a New Dual-input Impedance-based DC–DC Converter for Hybrid PV-FC Systems

Pezhman BAYAT, Alfred BAGHRAMIAN
Department of Electrical Engineering, Faculty of Engineering, Guilan University, Rasht, Iran
alfred@guilan.ac.ir

***Abstract*—A new dual-input DC-DC converter based on quasi-Z source converter is proposed in this study. This converter is a suitable option for efficiently interfacing two energy sources with a common load. The proposed topology, by integrating the switched-capacitor cell and coupled-inductor, provides a high step-up gain of voltage conversion at small duty cycles. This topology works only by two switches and voltage stress across the switches is low. Furthermore, continuous input current is one of the key features of the proposed converter which makes it suitable for hybrid photovoltaic and fuel cell systems. In this research, it is attempted to explain the operating principles, steady-state analysis, control and modulation for the proposed converter under continuous inductor current mode. The merits of the proposed converter are presented compared with those of other dual-input converters. Finally, simulation results from MATLAB\Simulink are presented and experiments with a 150W prototype are performed to investigate the performance and effectiveness of the studied circuit.**

***Index Terms*—control design, DC-DC power converter, fuel cells, photovoltaic systems, switched capacitor circuits.**

I. INTRODUCTION

In recent years, renewable energy sources have played a relatively important role in world energy production. However, intermittent and randomness of such energy sources may negatively impact the power grids [1]. In this regard, the hybrid energy systems (HESs) are installed to deal with these problems and also provide energy flow and voltage regulation among different inputs [2]. In general, HESs are classified into two categories: active and passive [3]. The passive HES for two input sources is shown in Fig. 1(a). In this structure, it is possible to only control the total power drawn from the combination of inputs, while there is no control over the power of each input. In addition, the contribution of each source is determined by its internal impedance. The active HES for two inputs is presented in Fig. 1(b). In this structure, the total power demand is distributed in a controlled manner between input sources using two separate single-input converters (SICs). Unlike the passive HES, voltages of input sources are not dependent on each other and thus the capacity of each input can be fully utilized. However, due to the use of an additional converter, which leads to higher cost and lower efficiency, these topologies turn into inefficient methods [4].

Multi-input converters (MICs) have recently appeared as promising approaches capable of interfacing with different inputs such as fuel cell (FC), renewable energy sources, and energy storages. The active HES using an MIC for two input sources is presented in Fig. 1(c). The key advantages of this type of converter are lower part counts, compact structure, and higher efficiency [5-6]. The fundamental concepts for developing SICs can be extended to the synthesis of MICs.

In the past decade, the isolated and non-isolated types of MICs have been widely reported in the literature. Non-isolated MICs are mainly used in the applications where a low voltage regulation ratio is required and isolation is not critically needed. These topologies are usually constructed by combining several traditional converters [7-12]. Based on this structure, some boost converters were combined in [7-8], some buck converters were connected at the input side in [9-10] and some buck-boost converters were utilized in [11-12]. Further, another two non-isolated MICs were presented in [13-14]. These two converters are suitable for the power management of renewable energy applications. However, simultaneous power delivery is not possible from input sources.

Notably, many applications require isolation in the system, which makes the non-isolated topologies insufficient. In applications that require isolation and high voltage gain ratios, isolated MICs are preferred [15]. As can be inferred from [15-18], isolated MICs are usually derived from the traditional full-bridge (FB) or half-bridge (HB) topologies, which use a large number of switches and high-frequency transformer (HFT). However, using HFT and a large number of switches increases the converter size, losses, and cost; makes the converter bulky; and reduces the overall power density.

The FB converter is one of the traditional topologies based on using galvanic isolation. Utilizing this structure, two types of isolated dual-input DC-DC converters were presented in [15-16] for photovoltaic (PV) applications. Topology proposed in [15] is derived by applying two-winding HFT. By sacrificing the isolation between the voltage sources on the same side of the isolation HFT, the number of switches in this category of topologies is reduced, simplifying its design. A similar topology, using FB and HB structures at both primary and secondary sides of the isolation transformer, was proposed in [16]. The authors in [17-18] offered a new isolated FB based MIC and attempted to use only one switch for each input source on the primary side. However, each input still requires a separate inductor, which increases the number of components in the topology. Topologies proposed in [15-18] are extraordinary for applications that require isolated port; however, there are still too many components and switches in these converters.

Digital Object Identifier 10.4316/AECE.2019.04006

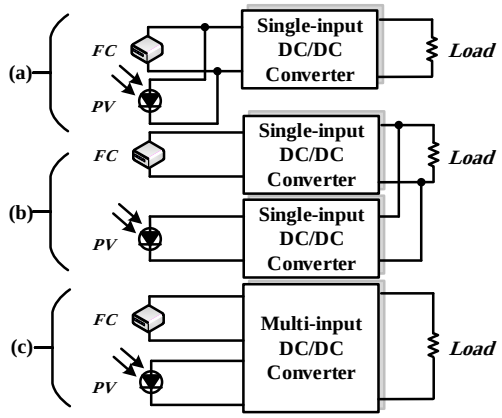

Figure 1. HESs: (a) passive topology using a SIC; (b) active topology using independent SICs; and (c) active topology using an MIC

Shoot-through is another common problem that may occur in these converters [19]. It is defined as the condition when both switches in one leg are turned ON, which leads to connection of input sources to the ground. Although control methods can be used to avoid shoot-through, this problem still exists and cannot be solved completely [20].

Impedance networks (INs) have been recently introduced as a new approach for improving the efficiency of SICs [21]. The main advantage of impedance based converters is to achieve higher voltage gain at a lower duty cycle and at lower losses [21-22]. Among these converters, the quasi Z-source converter (QZSC) has been presented recently with many key advantages, such as having low voltage stress on capacitors and continuous input current, which make it possible to improve the system reliability [22]. Nevertheless, this converter has a limited voltage gain, which makes it unusable for applications that require high voltage gain. More importantly, because of having the quasi Z-network, this topology is protected from shoot-through and open-circuit faults that will definitely damage converters. In [22], the traditional single-input QZSC was used for a PV power generation system. It showed excellent performance and fulfilled all the requirements for PV systems. However, for HESs, because this converter has only one input, first input must be connected to the load through this topology and then the second input must be connected through another SIC. As mentioned earlier, the main problem in this traditional method is that it has a low performance since an additional DC-DC converter is used for the second input.

According to the mentioned points, the main weakness of non-isolated MICs is that they are not suitable in applications where the system requires galvanic isolation; moreover, they have limited voltage gain. On the other hand, the main disadvantage of isolated MICs is the shoot-through problem and as well as the high number of components and switches in these converters.

This paper proposes a novel dual-input impedance-based DC-DC converter for hybrid PV-FC systems with the aim of filling the mentioned gap in the literature. The circuit configuration of the proposed converter is illustrated in Fig. 2. The proposed topology has dual inputs; one input is for the PV panel and the other input for the FC module. Consequently, it can transfer energy from both input sources to the output load individually and simultaneously. The presented topology integrates both the switched-capacitor and coupled-inductor techniques to achieve high voltage gains at rather small duty cycles with low voltage stress on components. In addition, it is immune to the shoot-through problem. Another feature of this typology is that there are only two switches in this structure. It is noteworthy that having a low number of switches leads to reduced losses, cost, and size of the converter and reduced the number of required gate driver circuits. Finally, an effective controlling mechanism has been developed for this converter.

The remainder of this paper is organized as follows: The structure of the proposed converter and its operating principles are presented in sections 2 and 3, respectively. Section 4 provides a short description of the steady-state analysis. Section 5 presents the efficiency analysis and power losses calculation. Comparison and performance assessment of the proposed converter with some other converters are discussed in section 6. Control, modulation, simulation, and experimental results for the proposed topology are presented in sections 7 and 8. Finally, in section 9, the concluding remarks are presented.

II. Topology Description of the Proposed Converter

The circuit of the proposed impedance-based dual-input DC-DC converter is shown in Fig. 2. This converter consists of one coupled-inductor with two windings. The coupled-inductor is modeled by magnetizing inductance L_m, an ideal transformer with turns ratio $N=N_S/N_P$ and leakage inductances L_{k1} and L_{k2}. In addition, the coupling coefficient is expressed by $\beta=L_m/(L_m+L_{k1})$. The circuit employs five diodes (D_{PV}, D_o, D_1, D_2, and D_3), one input inductor (L_1) and five capacitors (C_o, C_1, C_2, C_3 and C_4). Two power switches (S_1 and S_2) in the proposed structure are the main controllable components that control the power flow, where MOSFETs are used. In this structure, d_1 and d_2 are the duties of switches S_1 and S_2, respectively. The secondary side of the coupled-inductor with capacitors C_3 and C_4 and diodes D_2 and D_3 operates as a switched-capacitors cell. Then, higher voltage gains at rather small duty cycles are achieved without a further increase in the turns ratio of the coupled-inductor. Moreover, diode D_{PV} conducts in a complementary manner with switch S_2.

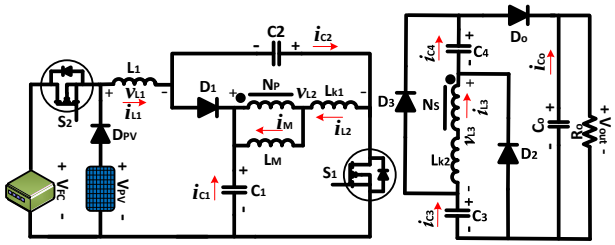

Figure 2. The proposed impedance-based dual-input DC-DC converter

III. Operational Principles

The proposed converter operates in continues conduction mode (CCM) condition. To simplify the circuit analysis, the following assumptions have been made:

- All devices consisting the power switches and diodes are assumed to be ideal;
- Due to the large enough values of all capacitors, their voltages can be assumed to be constant in one cycle;
- Due to the large enough values of input inductor (L_1), the input current ripple can be ignored in one cycle;
- Voltage of the FC module (V_{FC}) is greater than the

voltage of the PV panel (V_{PV}), therefore, one can obtain that $V_{PV} < V_{FC} < V_o$;

- Without loss of generality, the case $d_1 > d_2$ is assumed. For $d_1 < d_2$, a similar analysis can be followed.

The equivalent circuits depicting the operation of the proposed converter for each time interval and the theoretical waveforms diagram in CCM operation are respectively plotted in Fig. 3 and Fig. 4. Except time intervals III, IV and VII, other ones are very short so, these three intervals are the main switching modes during which the MOSFETs are ON or OFF for a long time. The proposed topology presents seven operation modes as shown in Figs. 3 and 4.

Time interval I ($t_0 < t < t_1$; Fig. 3(a)): At $t = t_0$, the switches S_1 and S_2 are turned ON, diodes D_2 and D_3 are forward biased, while the diodes D_1, D_{PV} and D_0 are reverse-biased. The capacitor C_2 is discharged. The magnetizing inductor (L_m) and leakage inductor (L_{k1}) are charged by V_{FC}. The energy stored in leakage inductor (L_{k2}) is transferred to switched-capacitor C_3 and C_4. The output capacitor C_o sustains the load.

Time interval II ($t_1 < t < t_2$; Fig. 3(b)): The switches S_1 and S_2 are remained ON during this period. Diode D_0 is forward biased and diodes D_1, D_2, D_3 and D_{PV} are reverse-biased, as clarified in Fig. 3(b). The capacitor C_2 and the leakage inductors keep their states as in time interval I. The energies stored in capacitors C_3 and C_4 are transferred to the load and also the output capacitor C_o is charged.

Time interval III ($t_2 < t < t_3$; Fig. 3(c)): In this mode, the energy from FC module is still transfer to L_m and L_{k1}, also the input inductor (L_1) receives energy from input source V_{FC}. Then, its current increases linearly. L_m transfers the stored energy to the secondary. The general conditions of the circuit are similar to the previous time interval. The energies stored in C_1 and C_2 are still discharged to the load. A part of magnetizing inductor energy is transferred to the secondary side through coupled-inductor and charging capacitors C_3 and C_4, with respect to the conversion ratio N, and also passes the energy to the load. The corresponding current waveforms are plotted in Fig. 4. When the switch S_2 is turned OFF at t_3, this interval is finished. Considering equivalent circuit shown in Fig. 3(c), by applying KVL principle, the following equations can be expressed as:

$$V_{L1}^{III} = V_{FC} + V_{C_2} \quad (1)$$

$$V_{L2}^{III} = V_{C_1} \quad (2)$$

$$V_{out} = V_{L3}^{III} + V_{C_3} + V_{C_4} \quad (3)$$

$$V_{Lm}^{III} = V_{L2}^{III} \times \frac{L_m}{L_m + L_{k1}} \quad (4)$$

Replacing coupling coefficient (β) in (4) and considering (2), V_{Lm}^{III} will be obtained as:

$$V_{Lm}^{III} = \beta V_{C_1} \quad (5)$$

Considering the turns ratio (N) of an ideal transformer, V_{L3}^{III} will be obtained as:

$$V_{L3}^{III} = N V_{Lm}^{III} \quad (6)$$

Applying V_{Lm}^{III} from (5) into (6), gives the following relationship for V_{L3}^{III} as:

$$V_{L3}^{III} = N \beta V_{C_1} \quad (7)$$

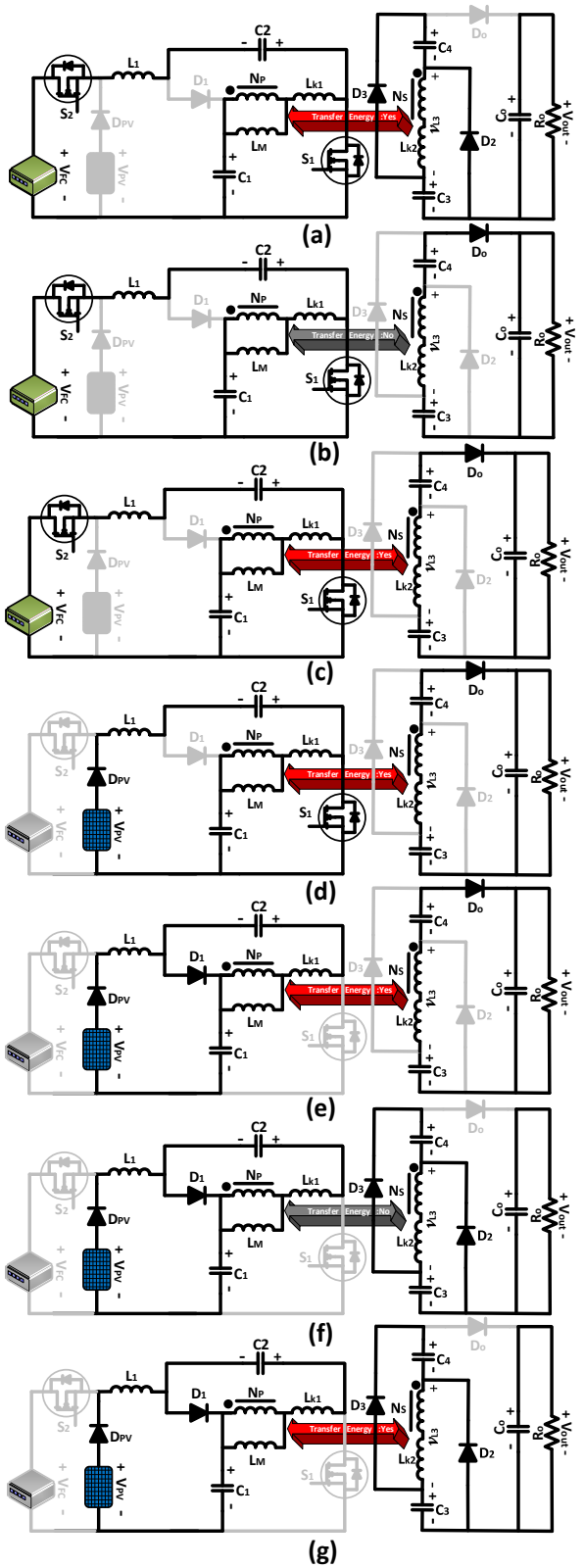

Figure 3. The operation modes of the proposed converter: (a) $t_0 < t < t_1$, (b) $t_1 < t < t_2$, (c) $t_2 < t < t_3$, (d) $t_3 < t < t_4$, (e) $t_4 < t < t_5$, (f) $t_5 < t < t_6$, (g) $t_6 < t < t_7$

Time interval IV ($t_3 < t < t_4$; Fig. 3(d)): It is similar to the previous time interval, but S_2 is turned OFF; the FC module is removed from the circuit and the energy from PV panel is transfer to L_m and L_{k1}. Because the primary side of the coupled-inductor is parallel with capacitor C_1, then, its current increases linearly with the same previous slope. Similar to previous time interval, V_{L3} and V_{L2} are equal to $-N\beta V_{C1}$ and V_{C1}, respectively. Therefore, following equations can be calculated using the circuit configuration

shown in Fig. 3(d) as follows.

$$V_{L1}^{IV} = V_{PV} + V_{C_2} \quad (8)$$

$$V_{L2}^{IV} = V_{C_1} \quad (9)$$

$$V_{L3}^{IV} = N\beta V_{C_1} \quad (10)$$

Time interval V ($t_4 < t < t_5$; Fig. 3(e)): At the moment t_4, S_1 is turned OFF, so both of the switches are OFF in this time interval; D_1 and D_o are forward biased and D_2 and D_3 are reverse-biased. L_{k2} transfers its energy to C_3, C_4 and the load. The capacitor C_o receives energy. This mode is terminated, when D_2 and D_3 conduct at $t = t_5$, as well as D_o is turned OFF.

Time interval VI ($t_5 < t < t_6$; Fig. 3(f)): At the moment t_5, diodes D_2 and D_3 are switched ON simultaneously. D_1 remained forward biased, while S_1 and S_2 and Do are OFF. In this stage, capacitors C_1, C_2 are charged. The energy transferred into the output load R_o transforms by discharged the output capacitor C_o.

Time interval VII ($t_6 < t < t_7$; Fig. 3(g)): In this mode, the diodes D_1, D_2, and D_3 conduct the current while switches S_1 and S_2 and diode D_o are OFF as in time interval VI. A part of magnetizing inductor energy is transferred to the secondary side through coupled-inductor and charging capacitors C_3 and C_4, with respect to the conversion ratio N. The corresponding current waveforms are plotted in Fig. 4. The output capacitor C_o solely supplies to the load. This mode is terminated, when S_1 and S_2 are turned ON at $t = t_7$. By applying KVL, the following equations can be calculated using the circuit configuration shown in Fig. 3(g).

$$V_{L1}^{VII} = V_{PV} + V_{C_2} + V_{L_2}^{VII} - V_{C_1} \quad (11)$$

$$V_{L2}^{VII} = -V_{C_2} \quad (12)$$

Substituting (12) into (11) leads to:

$$V_{L1}^{VII} = V_{PV} - V_{C_1} \quad (13)$$

Also following relationship is valid.

$$V_{L_3}^{VII} = -V_{C_3} = -V_{C_4} = NV_{Lm}^{VII} \quad (14)$$

Also:

$$V_{Lm}^{VII} = -\beta V_{C_2} \quad (15)$$

Substituting (15) into (14) leads to:

$$V_{C_3} = V_{C_4} = N\beta V_{C_2} \quad (16)$$

IV. Steady State Analysis

As mentioned earlier, due to the short values of time durations I, II, V and VI, they can be neglected. By writing down the voltage-second balance principle on the input and coupled inductors, the following equations are obtained.

The average voltage across V_{L2} during each switching cycle is given by:

$$\int_0^{T_s} V_{L_2} dt = 0 \quad (17)$$

Substituting (2), (9) and (12) into (17) leads to:

$$\int_0^{d_2T_s} V_{L_2}^{III} dt + \int_0^{(d_1-d_2)T_s} V_{L_2}^{IV} dt + \int_0^{(1-d_1)T_s} V_{L_2}^{VII} dt = 0$$
$$\Rightarrow d_2 V_{C_1} + (d_1 - d_2)V_{C_1} + (1-d_1)(-V_{C_2}) = 0 \quad (18)$$

In terms of the above-mentioned analysis, it can be concluded that the relationship between V_{C1} and V_{C2} is:

$$V_{C_1} = \frac{(1-d_1)}{d_1} V_{C_2} \quad (19)$$

Replacing (19) in (7), V_{L3}^{III} will be obtained as:

$$V_{L3}^{III} = N\beta \left(\frac{1-d_1}{d_1}\right) V_{C_2} \quad (20)$$

The average voltage across V_{L1} during each switching cycle is given by:

$$\int_0^{T_s} V_{L_1} dt = 0 \quad (21)$$

Substituting (1), (8) and (13) into (21) leads to:

$$\int_0^{d_2T_s} V_{L_1}^{III} dt + \int_0^{(d_1-d_2)T_s} V_{L_1}^{IV} dt + \int_0^{(1-d_1)T_s} V_{L_1}^{VII} dt = 0$$
$$\Rightarrow d_2 V_{FC} + (1-d_2)V_{PV} + d_1 V_{C_2} + (d_1 - 1)V_{C_1} = 0 \quad (22)$$

From (19) and (22) it can be consider that:

$$V_{C_2} = \frac{d_2 d_1}{1-2d_1} V_{FC} + \frac{d_1(1-d_2)}{1-2d_1} V_{PV} \quad (23)$$

Finally, considering (3), (16), (20), and (23), the voltage gain relationship will be obtained as:

$$V_{out} = N\beta \left[\frac{(1+d_1)(1-d_2)V_{PV} + d_2(1+d_1)V_{FC}}{1-2d_1} \right] \quad (24)$$

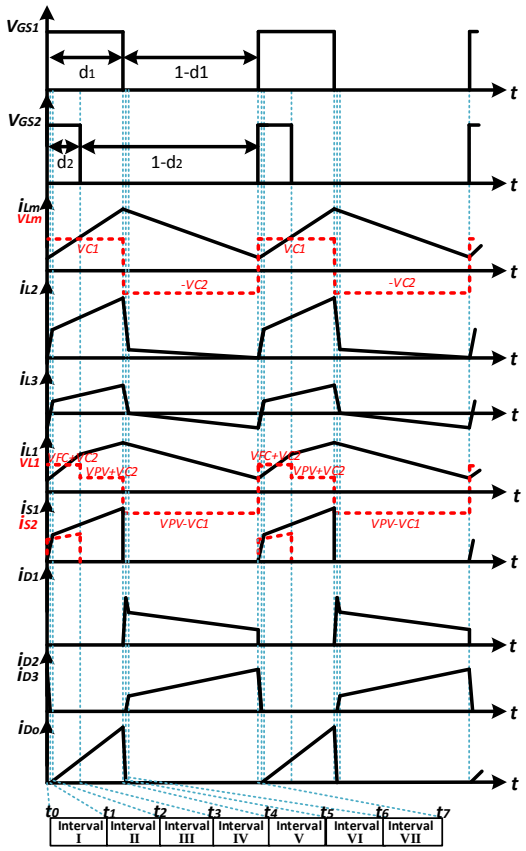

Figure 4. The typical waveforms of the proposed dual-input converter

Taking into account the conditions of input sources or failure protection, the proposed topology can operate in the single-input state. In this operation mode, the MOSFET S_2 is always kept ON or OFF, and the switching states are just for S_1 with duty cycle of d_1. When the MOSFET S_2 is kept ON, since the voltage of FC module is greater than the PV voltage, diode D_{PV} is always reverse-biased. Also on the other side, when the MOSFET S_2 is kept OFF, diode D_{PV} is always forward-biased. There are six operation modes in

one switching cycle and the equations in single-input state are exactly the same as that in the dual-input state. The only difference is a one stage charging of inductor L_1. Therefore in this mode, the time intervals I, II, III, IV, V and VI are similar to the time intervals I, II, III, V, VI and VII in dual-input mode, respectively. Consequently, by putting d_2=1 and d_2=0, in (24), the voltage gain relationship will be simplified as (25) and (26) respectively.

$$V_{out} = N\beta\left[\frac{1+d_1}{1-2d_1}\right]V_{FC} \quad (25)$$

$$V_{out} = N\beta\left[\frac{1+d_1}{1-2d_1}\right]V_{PV} \quad (26)$$

In both single-input and dual-input states, the voltage gain is a function of duty cycles (d_1 and d_2), turns ratio (N), and coupling coefficient β. The effect of β on voltage gain is very small. So, assuming that β=1, the ideal output voltage for different operational modes, can be plotted as in Fig. 5.

Also the voltage gain (V_{out}/V_{FC}) for single-input state is shown in Fig. 6. From this figure it can be conclude that, the voltage gain is increased exponentially and proportionally versus duty cycle (d_1) and turns ratio (N), respectively.

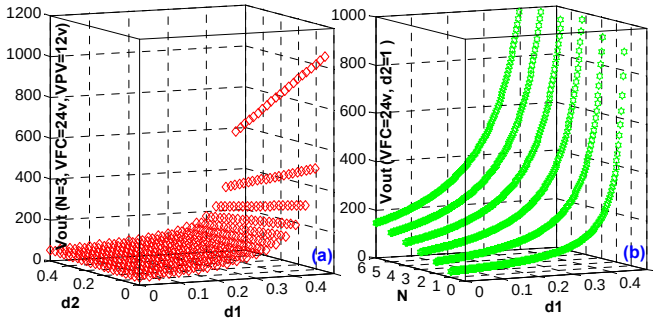

Figure 5. Output voltage for different operational modes (all voltages are in volt): (a) V_{out} for dual-input state, (b) V_{out} for single-input state

A. *Voltage stress of the components*

From the steady-state operation, according to Fig. 3(g), the voltage stress on the switch S_1 is given by:

$$V_{S1}^{ds} = V_{PV} + V_{C_2} - V_{L_1}^{VII} \quad (27)$$

Substituting (13) into (27), and considering (19), it is proved that:

$$d_1 \times V_{S1}^{ds} = V_{C_2} \quad (28)$$

Substituting (23) into (28), the following equation is derived as:

$$V_{S_1}^{ds} = \frac{(1-d_2)V_{PV} + d_2 V_{FC}}{1-2d_1} \quad (29)$$

Following the same concept, the voltage stress on the switch S_2 is constant and given by:

$$V_{S_2}^{ds} = V_{PV} + V_{FC} \quad (30)$$

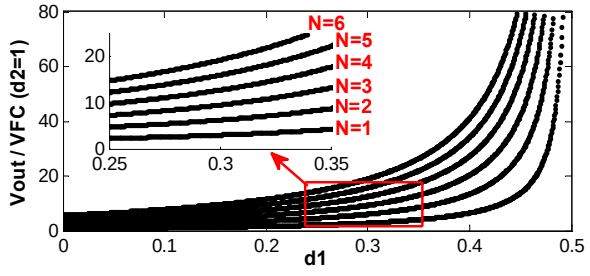

Figure 6. Voltage gain (V_{out}/V_{FC}) for single-input state

Figs. 3(c) and (g) are used for extracting the blocking voltage (BV) values V_{D1}, V_{D2}, V_{D3} and V_{Do} of the diodes D_1, D_2, D_3 and D_o.

From Fig. 3(c), it can be concluded that:

$$V_{D_1}^{BV} = V_{FC} - V_{C_1} - V_{L_1}^{III} \quad (31)$$

Substituting (1) into (31), and considering (19) and (23), it is proved that:

$$V_{D_1}^{BV} = -(V_{C_1} + V_{C_2}) = -\left[\frac{(1-d_2)V_{PV} + d_2 V_{FC}}{1-2d_1}\right] \quad (32)$$

Also:

$$V_{D_2}^{BV} = V_{C_3} - V_{out} \quad (33)$$

Considering (16), (23) and (24), and the relation $V_{D_2}^{BV} = V_{D_3}^{BV} = V_{D_o}^{BV}$, (33) is simplified as follows.

$$V_{D_2}^{BV} = V_{D_3}^{BV} = V_{D_o}^{BV} = -N\beta\left[\frac{(1-d_2)V_{PV} + d_2 V_{FC}}{1-2d_1}\right] \quad (34)$$

To closely examine the voltage stress of the components, Fig. 7 is extracted from (16), (19), (23), (29), (30), (32) and (34), for dual-input state. From Fig. 7, since the voltage stress of all switches is low, MOSFETs with low voltage stress and consequently low conduction loss can be used. In overall, it can be concluded that the voltage stresses of the components are function of d_1, d_2, N and β, as well as, input voltage of the sources.

V. Power Losses Calculation and Efficiency Analysis

In this section, a power loss model is developed. This power loss model calculates the losses in each component, e.g. switches, diodes, capacitors and inductors and computes the theoretical efficiency. In the proposed converter both the switches are MOSFET. Switch losses consist of conduction losses (P_{CL}^{L}) and switching (P_{ON-OFF}^{L}) [23]. Consequently, the total power losses of one MOSFET can be calculated as follows:

$$P_{Switches}^{L} = P_{CL}^{L} + P_{ON-OFF}^{L} \quad (35)$$

The conduction losses originate from the resistance of the switch during conduction time ($r_{ds(on)}$), which can be calculated from the following equation.

$$P_{CL}^{L} = r_{ds(on)} I_{SW(RMS)}^{2} \quad (36)$$

The switching losses of the switches can be derived as follows [23]:

$$P_{ON-OFF}^{L} = \frac{1}{6T_s}(V_{m,Si})(I_{avr,on})(t_{on} + t_{off}) \quad (37)$$

Where $V_{m,Si}$ and $I_{avr,on}$ are OFF-state maximum voltage and ON-state average current that each switch experiences during one switching cycle, respectively.

The power losses of the diodes are related to the conduction resistive (r_D) and their forward voltage drop (V_F) which can be obtained as:

$$P_{Diodes}^{L} = r_D I_{D,rms}^{2} + V_F I_{D,avr} \quad (38)$$

Where $I_{D,avr}$ and $I_{D.rms}$ are average and root mean square currents of each diode, respectively.

The power losses in the capacitors are caused by equivalent series resistances (r_c), which can be calculated as:

$$P_{Capacitors}^{L} = r_c I_{c,rms}^{2} \quad (39)$$

The power losses in the input and coupled inductors can be expressed as follows:

$$P_{Inductors}^{L} = r_L I_{L,rms}^2 + P_{core}^{L} \quad (40)$$

Where r_L is equivalent series resistance and $I_{L.rms}$ is root mean square current of input inductor.

The total power loss in the proposed converter by considering above conditions can be calculated as follows:

$$P_{Loss}^{tot} = P_{Switches}^{L} + P_{Diodes}^{L} + P_{Inductors}^{L} + P_{Capacitors}^{L} \quad (41)$$

The input power, output power and the converter efficiency can be calculated, respectively, from (42)-(44).

$$P_{Inputs} = P_{Output} + P_{Loss}^{tot} \quad (42)$$

$$P_{Output} = V_O I_O \quad (43)$$

$$\eta = \frac{P_{Output}}{P_{Inputs}} \times 100 \quad (44)$$

The theoretical calculated efficiency of the proposed dual-input converter under different output loads is shown in Fig. 8. The proposed converter has maximum about %95.5 efficiency in dual-input state and also has a good performance in a wide output power range. It must be noticed that, the dominant losses occur in the coupled-inductor, the diodes and the switches, respectively.

VI. Comparison and Performance Assessment

Table I shows a comparative study of some critical parameters between the proposed and similar dual-input converters. References [7-8],[10],[13],[15-16] have been selected to achieve this purpose. In this comparison, component count, input current ripple and stress on the input sources are taken in account. Converters in [8],[10],[13],[15] are without any coupled-inductor or any HFT, while the other competitors are used coupled-inductor or HFT for increasing voltage gain. The voltage gain ratio of the proposed topology is higher than the others at duty cycle range only between $0<d_1<0.5$. Consequently, due to combination of the quasi Z-source network with switched-capacitors technique, realizing higher voltage gains at rather small duty cycles is achieved without further increase of the turns ratio of coupled-inductor. The turns ratio of the coupled-inductor of mentioned-MICs is assumed to be equal to 3. Input current ripple is also very important in the application of PV/FC systems. So, from the perspective of input current quality, the converter in [10] and the proposed converter, which employed an additional inductor at their input port, lead them to have a low ripple continuous current at their input stage. Therefore, compared with other mentioned-converters, these two topologies put lower stress on the input voltage sources. In terms of the number of components, the total number of inductors, capacitors and the total number of switches are approximately less or equal than the other mentioned-MICs. It is noteworthy that, less number of switches leads to reduced size, cost and losses of converter and also reduced number of required gate driver circuits and consequently higher efficiencies. The maximum efficiency of the proposed topology with V_O=79V, V_{PV}=12V and V_{FC}=24V in dual-input state is about %95.5. In overall, by considering detailed comparisons in the Table I, it can be concluded that the proposed topology has relatively better performance than other aforementioned converters.

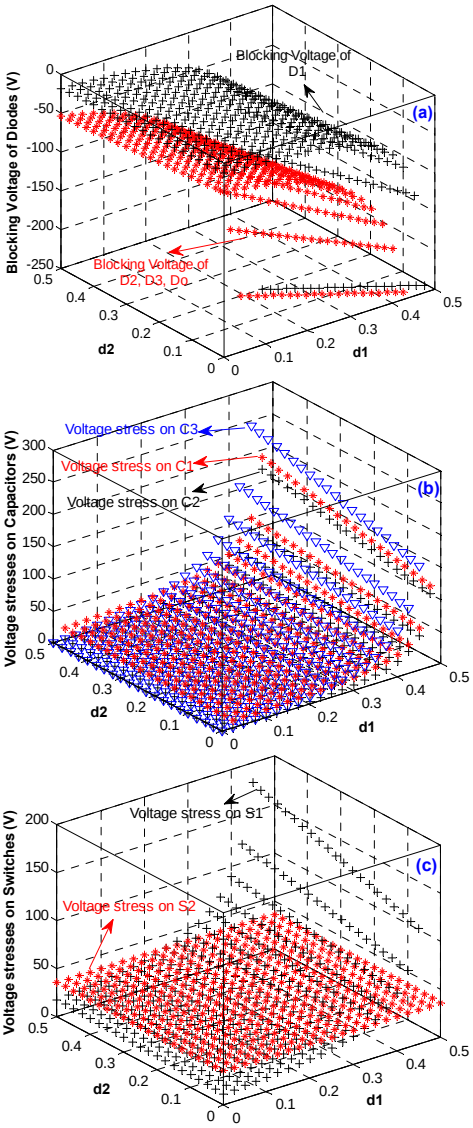

Figure 7. Voltage stress of the components: (a) Diodes, (b) Capacitors, (c) Switches

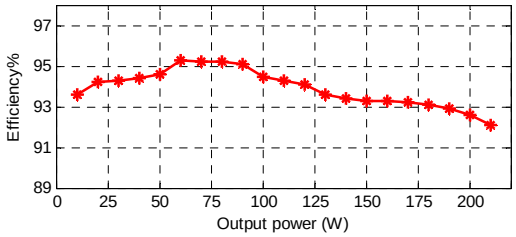

Figure 8. Theoretical calculated efficiency versus output power of the proposed topology

TABLE I. Features Comparison of Related Dual-Input Converters with Proposed Topology

Refs.	Types	Components					Input current ripple	Stress on the input sources
		Switches	Diodes	Capacitors	Inductor	Coupled inductor/HF		
[7]	Non-Isolated	3	5	6	1	1	Moderate	Large
[8]	Non-isolated	5	3	1	1	0	Moderate	Large
[10]	Non-isolated	2	2	1	1	0	Small	Small
[13]	Non-isolated	4	2	1	1	0	Moderate	Large
[15]	Isolated	3	2	3	2	1	Large	Large
[16]	Isolated	7	0	3	1	1	Large	Large
Proposed converter	Isolated	2	5	5	1	1	Small	Small

VII. Control and Modulation

The modified version of power management strategy for PV power systems proposed in [24] is applied to the proposed converter, considering that the modulation strategies of different topologies are usually different. In doing so, the power management strategy, PWM modulation and control circuit of the proposed converter are drawn in Figs. 9 and 10. Three proportional-integral (PI) regulators, PV voltage regulator (PVVR) for regulate the PV panel voltage to its reference value, FC voltage regulator (FCVR) for FC voltage control and output voltage regulator (OUTVR) for output voltage control, are selected to implement the control system. Indeed, output voltage (V_{out}), PV panel voltage (V_{PV}) and FC voltage (V_{FC}) are feedback to track their references, $V_{out\text{-}ref}$, $V_{MPP\text{-}PV}$ and V_{MPP_FC}, respectively. In order to design three PI controllers for the proposed converter, the small-signal model should be obtained first [25]. This model can demonstrate the converter transient behavior and its stability, and facilitates proper design of the converter controller. After that, by extracting the transfer functions, the system dynamics can be easily investigated through frequency domain (Bode plot). Consequently, designing the compensators for the control loops is simplified. From Fig. 3, the power flow through both the PV port and FC port can be controlled with d_2. In fact, when S_2 is ON, FC transfers energy to the load and on the other hand, when S_2 is OFF, PV panel supplies the load. Therefore, d_2 is selected as the control input when realizing the PVVR and FCVR loops. In the control strategy, maximum power point tracking (MPPT) methods are used for both PV and FC ports. The reference value for PV panel ($V_{MPP\text{-}PV}$) is generated by an MPPT method using perturb and observe (P&O) algorithm [26]. Otherwise the reference value for FC module (V_{MPP_FC}) is generated by a simple MPPT method using voltage based technique [27]. The voltage based MPPT technique for FC module expresses that there is a liner relation between voltage in maximum power point and $V_{OC\text{-}FC}$ (open-circuit voltage). Therefore, $V_{MPP\text{-}FC}= K_v \times V_{OC\text{-}FC}$; where K_v is voltage factor and it has been brought in different module temperature. Indeed, by increasing the temperature, K_v is decreasing and the variation of this parameter with respect to temperature is linear and slop of variation is approximately constant [27]. However, according to the inherent power balance in a dual-input converter, only two of the three ports (PV, FC and output ports) can be regulated simultaneously [24]. On the other, as output voltage regulation is usually mandatory, only one of the input regulators can be implemented at a time. In order to avoid the sudden transition between each input regulator, the selection of them is based on the minimum competition logic proposed in [24], as shown in Fig. 10. Based on this method, PV port is operated under PVVR most of the time. Therefore, FCVR would not be active under normal operation. FCVR will start to take control over d_1 only when FC maximum voltage setting ($V_{max\text{-}FC}$) is reached and FCVR output ($V_{C\text{-}FCVR}$) goes down to win the minimum function; Therefore, FC voltage (V_{FC}) is feedback to track its maximum power point reference ($V_{MPP\text{-}FC}$). Moreover, once FCVR starts to take control over d_2, PVVR will be disabled immediately to avoid the noise issue caused by the MPPT algorithm. Again, after controlling FC output voltage, in order to achieve maximum power from the PV panels, PVVR will start to take control over d_2, instantly. In a nutshell, since the voltage based MPPT technique for FC is only temperature dependent and FC modules are much more robust than PV panels, therefore, PVVR will be more involved and it will have a greater participation than FCVR. Consequently, under dual-input state, with regards to FC output voltage, only one of two loops (PVVR and FCVR) will be active at a time. So, whether d_2 is commanded by PVVR and FCVR depends on the conditions. From (25) and (26), the output voltage in single-input state is controlled by d_1; also from (24) in dual-input state, it is controlled by both d_1 and d_2. In doing so, d_1 is selected as the control input when realizing the OUTVR loop for generality. It should be noted that, in the single-input state, at least one of the two inputs is in the circuit, so d_2 is 1 or 0 and d_1 is only used as the control input. Therefore, in this state only the OUTVR is active.

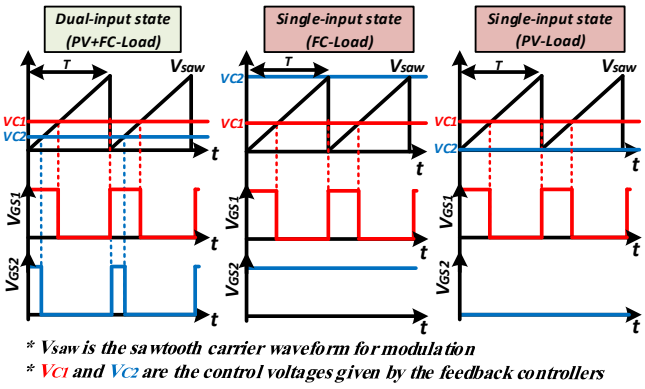

Figure 9. PWM modulation in different working states

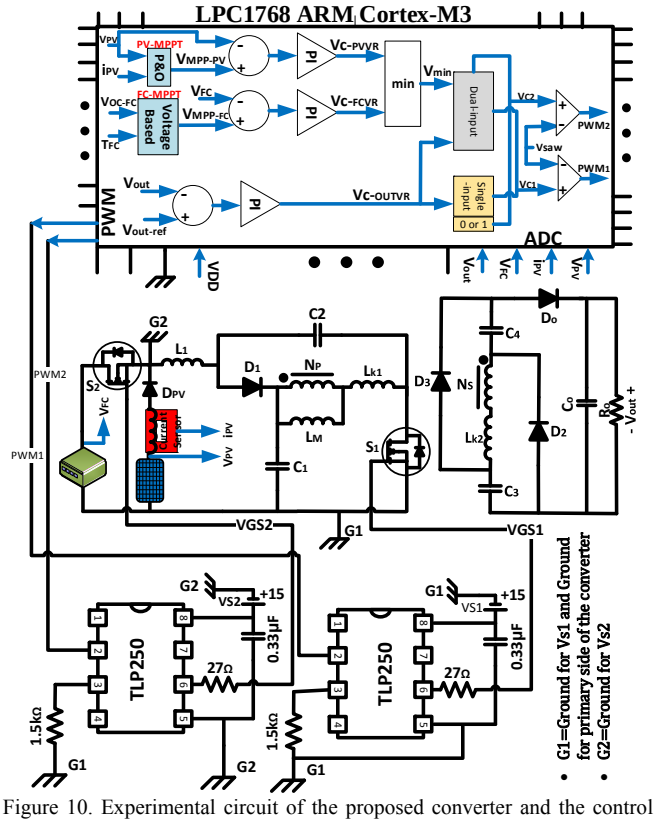

Figure 10. Experimental circuit of the proposed converter and the control strategy in different working states

The control signals $V_{C\text{-}PVVR}$, $V_{C\text{-}FCVR}$ and $V_{C\text{-}OUTVR}$ are generated from three PI regulators and for dual-input and

single-input states, S_1 and S_2 should be controlled by different gating signals as follows:

- In dual-input state, PVVR and FCVR run in parallel to compete for minimum value in order to win control over d_2 [24]. Therefore V_{min} should control S_2 and $V_{C\text{-}OUTVR}$ should control S_1. According to the Fig. 9 and also Fig. 10, $V_{C2}=V_{min}$, and V_{C1} is determined by $V_{C\text{-}OUTVR}$, regarding that, $V_{saw}>V_{C1}>V_{C2}$.
- In single-input state (FC-load), $V_{C\text{-}OUTVR}$ should control S_1, whereas S_2 should be constant ON. According to the Figs. 9 and 10, $V_{C2}=1$, therefore V_{C1} is determined by $V_{C\text{-}OUTVR}$, regarding that, $V_{saw}> V_{C1}$.
- In single-input state (PV-load), $V_{C\text{-}OUTVR}$ should control S_1, whereas S_2 should be constant OFF. According to the Figs. 9 and 10, $V_{C2}=0$, therefore V_{C1} is determined by $V_{C\text{-}OUTVR}$, regarding that, $V_{saw}> V_{C1}$.

VIII. Simulation and Experimental Results

In this section, simulation and experimental results are demonstrated to investigate the performance and effectiveness of the proposed converter. Simulations are done in the MATLAB/Simulink environment and simulation parameters are listed in Table II. To provide good visualization, simulation waveforms are presented with the timescale. According to the equipment availability in the lab, as well as for the sake of safety, a topology supplied by a low input voltage has been tested. For this reason, for both simulation and experimental results, V_{PV} and V_{FC} are considered to be 12V and 24V, respectively and the switching frequency is set to 30 kHz. For dual-input state, the voltage/current waveforms of input and magnetizing inductors (I_{L1}, V_{L1}, I_{LM} and V_{LM}), diodes (I_{D1}, I_{D2}, I_{D3} and I_{DO}) and load (I_{out} and V_{out}) obtained from simulations have been illustrated in Fig. 11. It is critical to note that, Fig. 11 is consistent with the theoretical analysis shown in Fig. 4.

To confirm the simulation results and also to corroborate the performance and effectiveness of the proposed converter, a 150W prototype has been implemented in the laboratory with the same circuit parameters as those used in the former as depicted in Table II. Fig. 12 shows a photograph of the experimental system.

As illustrated in Figs .10 and 12, a LPC1768 ARM Cortex-M3 microcontroller was used for implementing control and modulation strategy and feeding appropriate gate signals. Analog-to-digital (ADC) unit has been used in the sensing system of the controller. Finally two PWM signals are generated with various duty cycles at the same frequency. After that, the generated signals are isolated with TOSHIBA photocoupler (TLP250) to produce + 15 and 0 V for turning the MOSFETs ON and OFF. The PV and FC voltages are generated by the RE-104-ABZARAZMA module. The voltage waveforms were obtained using differential probe type GDP-025, also the current waveforms were measured with a current probe of type GCP-100. Diodes D_2, D_3 and D_o are ultrafast with maximum V_F=1.75V while diodes D_1 and D_{PV} are schottky with maximum V_F=2.1V. Additionally, the lab available MOSFET IRFP4668 with low ON resistance 8mΩ and turn-off delay time 64ns is used for the switches. The core type of the input inductor is iron powder toroidal core (33×26×10), while ferrite core EE35/42/12 with 0.3 mm air gap is used for coupled-inductor. The primary and secondary windings of the coupled-inductor had 18 and 54 turns, respectively. The magnetizing inductance measured from the primary side was 150uH. The leakage inductance measured at the primary winding by shorting the secondary winding was 1.5uH. Similarly, the leakage inductance measured at the secondary winding by shorting the primary winding was 1.5uH.

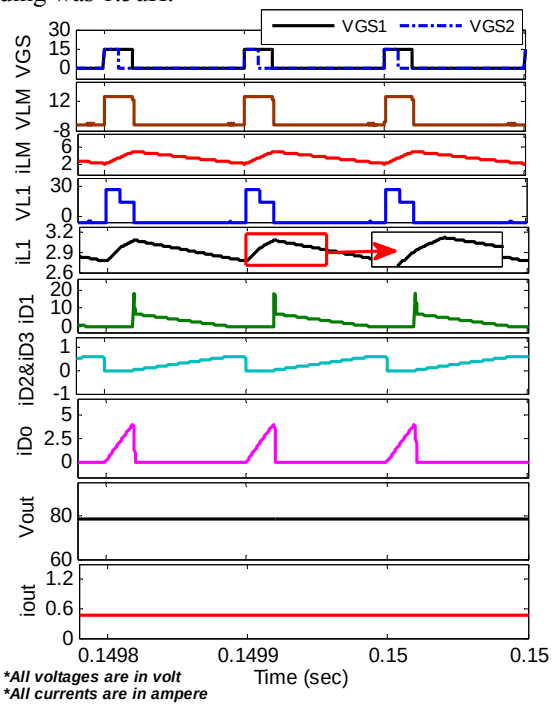

Figure 11. Simulation results for the proposed converter: PWM gate pulses, voltage/current waveforms of input and magnetizing inductors (I_{L1}, V_{L1}, I_{LM} and V_{LM}), diodes (I_{D1}, I_{D2}, I_{D3} and I_{DO}) and load (V_{out} and I_{out})

Table II. Simulation and Experimental Parameters

Parameters	Values	
Input voltage (V_{PV})	12V	
Input voltage (V_{FC})	24V	
Load (R_o)	150Ω (150W)	
Switching frequency (f_s)	30KHZ	
Input inductor (L_1)	500uH-iron powder toroidal core (33×26 ×10)	
Coupled-inductor	L_m	150uH
	L_{k1} and L_{k2}	1.5uH
	Turns Ratio N(N_p:N_s)	3(18:54)
	Core (Ferrite)	EE35/42/12
Capacitors C_1 and C_2	330uF (200V)	
Capacitors C_3 and C_4	15uF (400V)	
Capacitor C_o	680uF (450V)	
Power switches S_1 and S_2	IRFP4668 with R_{DS}(ON)=8mΩ	
Diodes D_2, D_3 and D_o	MUR4100E with maximum V_F=1.75V	
Diodes D_1 and D_{PV}	RUR30120 with maximum V_F=2.1V	
Microcontroller	LPC1768 ARM Cortex-M3	
Output voltage ref. ($V_{out\text{-}ref}$)	79V and 144V (for dual-input and single-input states)	

In practice, two separate tests (dual-input and single-input states), were conducted in order to verify the feasibility of operation modes and steady state validation of the proposed converter. Therefore, the voltage/current waveforms of input and magnetizing inductors (I_{L1} and I_{LM}), diodes (I_{D1}, I_{D2}, I_{D3} and I_{DO}), load (I_{out} and V_{out}), capacitors (V_{C1}, V_{C2}, V_{C3} and V_{C4}) and the PWM gate pulses obtained from experimental results have been illustrated in Figs. 13 and 14.

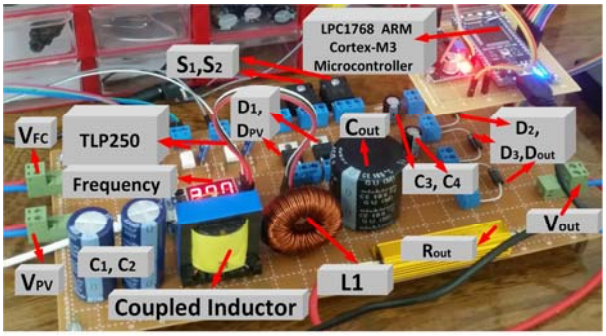

Figure 12. Photograph of experimental setup

Experimental results for dual-input state are depicted in Fig. 13. Apparently, the calculated values from (17)-(24) are in consistent with the experimental results. For this mode, from Fig. 13, one can obtain that the output voltage V_{out} is within (79.4V,79.8V), the input inductor current I_{L1} is within (2.8A,3.2A), and magnetizing inductor current I_{Lm} is within (2.2A,5.7A). Also, the ripples of the input inductor current Δi_{L1} and the magnetizing inductor current Δi_{Lm} are (3.2–2.8)/2=0.2A and (5.7–2.2)/2=1.75A, respectively. From Fig. 11, the simulation results are V_{out}=79V, I_{L1}=(2.65A,3.1A), I_{Lm}=(2A,6A), Δi_{L1}=(2.65–3.1)/2=0.225A, Δi_{Lm}=(6–2)/2=2A, respectively.

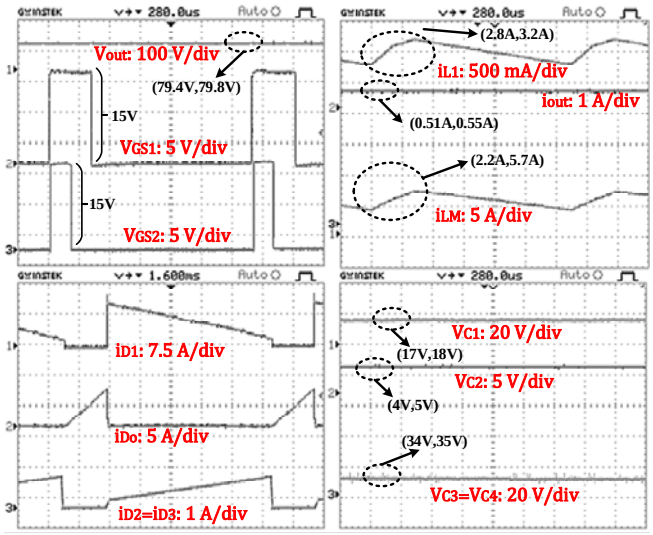

Figure 13. Experimental results of proposed converter for dual-input state

Experimental results for single-input state (PV panel is removed), are depicted in Fig. 14. It can be concluded that the proposed structure ensures output voltage regulation and also continuous current at the input port and confirmed that the proposed dual-input converter is suitable for the practical applications which requiring single-input state, to deal with different conditions.

The robustness of the proposed converter against the sudden variations in the input voltages is demonstrated in Fig. 15(a). In doing so, the PV and FC voltages are increased by nearly 40%, while the output voltage is constant (79V). This experiment confirmed that the proposed converter is resistant against the variation in the input voltages. Also, the robustness of the proposed converter is investigated through another experiment with a notable variation in output load (R_{out}=150→ 100) and result is shown in Fig. 15(b). From this result, the output voltage remains constant at its reference value, with only a small increase in the voltage ripples. Indeed, it can be concluded that the amount of voltage ripples are greater at higher loads. Meanwhile, when the load is increases, the output current should also be increased to provide output power.

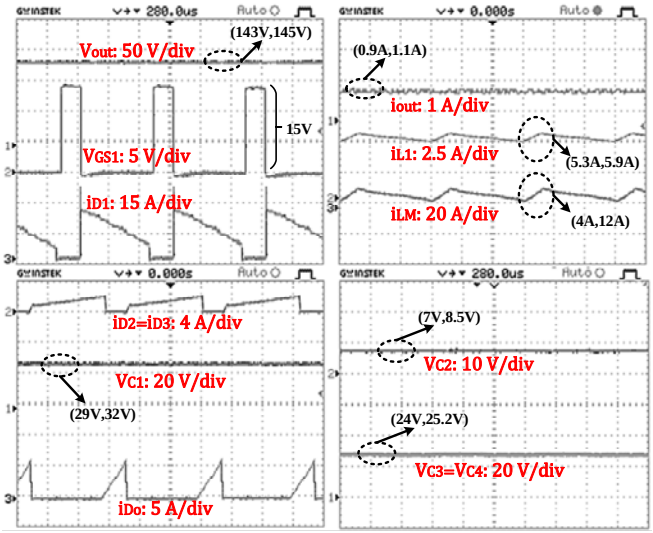

Figure 14. Experimental results of proposed converter for single-input state

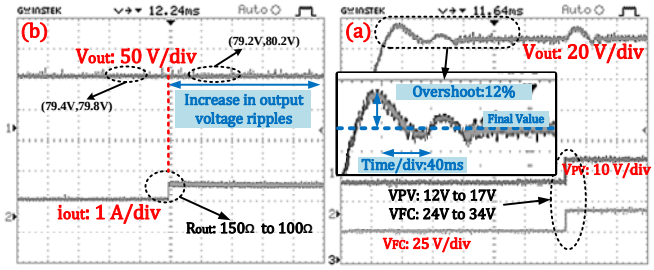

Figure 15. V_{out} of the proposed structure with respect to: (a) variations in the input voltages, (b) load variation

Table III is extracted from Figs. 11 and 13 and highlights the outcome of the numerical comparison between simulation results and experimental values. From this table, it is clear that the output voltage for dual-input state is successfully regulated at 79V in both experiment and simulation results. It is also observed that the mentioned-parameters in the both experiment and simulation results appear similar.

TABLE III. NUMERICAL COMPARISON BETWEEN SIMULATION AND EXPERIMENTAL RESULTS

Parameters	Simulation results	Experimental results
V_{out}	79V	(79.4V,79.8V)
I_{out}	0.526A	(0.51A,0.55A)
I_{L1}	(2.65A,3.1A)	(2.8A,3.2A)
Δi_{L1}	0.225A	0.2A
I_{LM}	(2A,6A)	(2.2A,5.7A)
Δi_{Lm}	2A	1.75A
$I_{D1,max}$	14A	13.25
$I_{D2,max}$= $I_{D3,max}$	0.8A	0.85A
$I_{Do,max}$	4.5A	5A
$V_{C1,avg}$, $V_{C2.avg}$	17.3V, 4.55V	17.5V, 4.5V
$V_{C3,avg}$= $V_{C4,avg}$	34.2V	34.5V

Finally, the efficiency of the built prototype under dual-input state is measured and plotted in Fig. 16. Compared with the theoretical calculated efficiency (Fig. 8), the measurement results are generally acceptable and it can be seen that the curves are in good agreement with each other, especially at medium load current range.

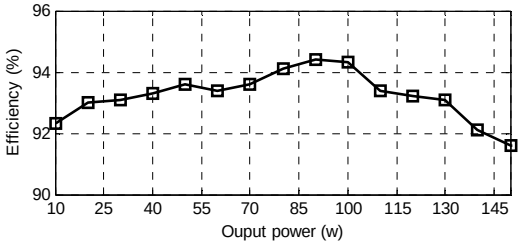

Figure 16. Measured results of efficiency from the built prototype

IX. Conclusion

In this paper, a novel impedance-based dual-input DC-DC converter has been proposed. The proposed converter inherits all the QZSC advantages such as having low voltage stress on capacitors, being immune to shoot-through problem and having continuous input current. Moreover, the proposed topology interfaces two different voltage sources by using only two switches. Applying switched-capacitor and coupled-inductor techniques, the voltage gain of the proposed converter is significantly improved. Furthermore, the proposed converter can provide energy to the load even if one of the power supplies fails to provide energy. The operation principles, steady-state analysis, control and modulation are explained in detail. In order to validate the theoretical analysis, the simulation studies have been conducted. Finally the experimental results are added to justify the feasibility of the proposed topology. It can be concluded that the proposed dual-input converter with the noted salient features can be an appropriate candidate for the power conversion of hybrid PV/FC systems.

References

[1] Y. K. Renani, B. Vahidi, H. A. Abyaneh, "Effects of Photovoltaic and Fuel Cell Hybrid System on Distribution Network Considering the Voltage Limits," Advances in Electrical and Computer Engineering, vol. 10, no. 4, pp. 143–148, 2010. doi:10.4316/AECE.2010.04023

[2] M. Venmathi, R. Ramaprabha, "Investigation on Fuzzy Logic Based Centralized Control in Four-Port SEPIC/ZETA Bidirectional Converter for Photovoltaic Applications," Advances in Electrical and Computer Engineering, vol. 16, no. 1, pp. 53–60, 2016. doi:10.4316/AECE.2016.01008

[3] P. Bayat, A. Baghramian, P. Bayat, "Implementation of hybrid electric vehicle energy management system for two input power sources," Journal of Energy Storage, vol. 17, pp. 423–440, 2018. doi:10.1016/j.est.2018.03.019

[4] Y. Li, X. Ruan, D. Yang, F. Liu, C. K. Tse, "Synthesis of multiple input DC/DC converters," IEEE Transactions on Power Electronics, vol. 25, no. 9, pp. 2372–2385, 2010. doi:10.1109/TPEL.2010.2047273

[5] A. Nahavandi, M. T. Hagh, M. B. Sharifian, S. Danyali, "A nonisolated multiinput multioutput DC–DC boost converter for electric vehicle applications," IEEE Transactions on Power Electronics, vol. 30, no. 4, pp. 1818–1835, 2015. doi:10.1109/TPEL.2014.2325830

[6] W. Jiang, B. Fahimi, "Multiport Power Electronic Interface - Concept, Modeling, and Design," IEEE Transactions on Power Electronics, vol. 26, no. 7, pp. 1890–1900, 2011. doi:10.1109/TPEL.2010.2093583

[7] L. Chien, C. Chen, J. Chen, Y. Hsieh, "Novel Three-Port Converter with High-Voltage Gain," IEEE Transactions on Power Electronics, vol. 29, no. 9, pp. 4693–4703, 2014. doi:10.1109/TPEL.2013.2285477

[8] A. Khaligh, J. Cao, Y. J. Lee, "A Multiple-Input DC–DC Converter Topology," IEEE Transactions on Power Electronics, vol. 24, no. 3, pp. 862–868, 2009. doi:10.1109/TPEL.2008.2009308

[9] F. D. Rodriguez, W. G. Imes, "Analysis and modeling of a two-input dc/dc converter with two controlled variables and four switched networks," in Proc. 31st Intersoc. Energy Convers. Eng. Conf., pp. 11–16, 1996. doi:10.1109/IECEC.1996.552892

[10] Y. M. Chen, Y. C. Liu, S. H. Lin, "Double-input PWM dc/dc converter for high/low voltage sources," IEEE Transactions on Industrial Electronics, vol. 53, no. 5, pp. 1538–1545, 2006. doi:10.1109/TIE.2006.882001

[11] B. Dobbs, P. Chapman, "A multiple-input dc–dc converter topology," IEEE Power Electronics Letters, vol. 1, no. 1, pp. 6–9, 2003. doi:10.1109/LPEL.2003.813481

[12] N. D. Benavides, P. L. Chapman, "Power budgeting of a multiple-input buck–boost converter," IEEE Transactions on Industrial Electronics, vol. 20, no. 6, pp. 1303–1309, 2005. doi:10.1109/TPEL.2005.857531

[13] A. Sivaprasad, G. K. Gangavarapu, S. Kumaravel, S. Ashok, "Performance Analysis of Novel Bridge Type Dual Input DC-DC Converters," IEEE Access, vol. 5, pp. 15340–15353, 2017. doi:10.1109/ACCESS.2017.2734328

[14] M. R. Banaei, H. Ardi, R. Alizadeh, A. Farakhor, "Non-isolated multi-input–single-output DC/DC converter for photovoltaic power generation systems," IET Power Electronics, vol. 7, no. 11, pp. 2806–2816, 2014, doi:10.1049/iet-pel.2013.0977

[15] J. Zeng, W. Qiao, L. Qu, "Modeling and Control of a Three-Port DC-DC Converter for PV-Battery Systems," in IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, USA, 2015. doi:10.1109/APEC.2015.7104586

[16] G. Feng, F. Lixing, Z. Xuan, Y. Chengcheng, L. He, W. Jin, "A Family of Quasi-Switched-Capacitor Circuit-Based Dual-Input DC/DC Converters for Photovoltaic Systems Integrated With Battery Energy Storage," IEEE Transactions on Power Electronics, vol. 31, no. 12, pp. 8237–8246, 2016. doi:10.1109/TPEL.2016.2519394

[17] J. Zeng, W. Qiao, L. Qu, "An Isolated Three-Port Bidirectional DC–DC Converter for Photovoltaic Systems with Energy Storage," IEEE Trans. Industry Applications, vol. 51, no. 4, pp. 3493–3503, 2015. doi:10.1109/TIA.2015.2399613

[18] G. J. Su, F. Z. Peng, "A low cost, triple-voltage bus dc/dc converter for automotive applications," in Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, pp. 1015–1021, 2005. doi:10.1109/APEC.2005.1453116

[19] X. Pei, S. Nie, Y. Kang, "Switch short-circuit fault diagnosis and remedial strategy for full-bridge DC–DC converters," IEEE Transactions on Power Electronics, vol. 30, no. 2, pp. 996–1004, 2015. doi:10.1109/TPEL.2014.2310201

[20] G. Zhang, B. Zhang, Z. Li, Y. Zhang, S. Chen, "A Novel Single-Input–Dual-Output Impedance Network Converter," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 3, pp.1133–1141, 2017. doi:10.1109/JESTPE.2017.2655510

[21] N. Zhang, G. Zhang, K. W. See, "A Δ-Y Hybrid Impedance Network Boost Converter with Reduced Input Current Ripple," IEEE Transactions on Power Electronics, vol. 33, no. 4, pp. 2803–2808, 2018. doi:10.1109/TPEL.2017.2751638

[22] D. Vinnikov, I. Roasto, "Quasi-Z-source based dc/dc converters for distributed power generation" IEEE Transactions on Power Electronics, vol. 58, no. 1, pp. 192–201, 2011. doi:10.1109/TIE.2009.2039460

[23] S. Dusmez, A. Hasanzadeh, A. Khaligh, "Comparative analysis of bidirectional three-level DC–DC converter for automotive applications," IEEE Transactions on Industrial Electronics, vol. 62, no. 5, pp. 3305–3315, 2015. doi:10.1109/TIE.2014.2336605

[24] Z. Zhou, H. Wu, X. Ma, Y. Xing, "A non-isolated three-port converter for stand-alone renewable power system," in IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society, 2012. doi:10.1109/IECON.2012.6389360

[25] Y. M. Chen, A. Q. Huang and X. Yu, "A high step-up three-port DC–DC converter for stand-alone PV/battery power systems," IEEE Transactions on Power Electronics, vol. 28, no. 11, pp. 5049-5062, 2013. doi:10.1109/TPEL.2013.2242491

[26] D. P. Hohm and M. E. Ropp, "Comparative study of maximum power point tracking algorithms using an experimental, programmable, maximum power point tracking test bed," in Proc. IEEE Photovoltaic Spec. Conf., pp. 1699–1702, 2000. doi:10.1109/PVSC.2000.916230

[27] Y. E. Song, H. C. Boghani, H. S. Kim, B. G. Kim, T. Lee, B. H. Jeon, G. C. Premier and J. R. Kim, 2016, "Maximum Power Point Tracking to Increase the Power Production and Treatment Efficiency of a Continuously Operated Flat-Plate Microbial Fuel Cell," Energy Technology, vol. 4, no. 11, pp. 1427-1434, 2016. doi:10.1002/ente.201600191