Design Time Temperature Reduction in Mixed Polarity Dual Reed-Muller Network: a NSGA-II Based Approach

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***Abstract*—Proposed work addresses the existing thermal problem of OR-XNOR based circuit by introducing design time thermal management technique at the logic level. The approach is used to reduce the peak temperature by eliminating local hotspots. In proposed thermal-aware synthesis, non-dominated sorting genetic algorithm-II (NSGA-II) based meta-heuristic search algorithm is used to select a suitable input polarity of Mixed Polarity Dual Reed-Muller Expansion (MPDRM) to reduce the power and power-density by optimizing the area sharing. A parallel tabular technique is used for input polarity conversion from Product-of-Sum (POS) to MPDRM function. Finally, the optimized solutions are implemented in the physical design level to obtain the actual values of area, power, and temperature. MCNC benchmark suit is considered for performance evaluation. A comparative study of the proposed approach with existing state-of-art algorithms such as fixed and mixed polarity Reed-Muller network is reported. A significant reduction in area occupancy, power dissipation, and peak temperature generation are reported.**

***Index Terms*—genetic algorithms, logic design, Pareto optimization, power dissipation, thermal analysis.**

I. INTRODUCTION

Excessive heat generation within the highly scaled integrated circuits (ICs) due to uneven distribution of power-density causes thermal aspects as important issue in low cost portable electronic gadgets. Peak temperature (hotspots) influences the reliability, packaging cost, cooling cost and performance of a device [1-2]. Most of the research work to minimize the thermal effect is addressed in physical design domain [3-5]. It is observed that with the increase of temperature due to the increase of power-density the cooling cost of a high performance processor rises exponentially i.e., $ 1-3 or more per watt of power dissipation [6]. So, temperature defining parameter (power-density) needs to be considered at higher levels of very large scale integration (VLSI) design flow (logic and circuit level) to improve the power and thermal characteristics such that cooling cost of IC is reduced and reliability of the IC is increased. Few literatures reported the effect of thermal issues and its probable solution [7-9]. Here, a study has been proposed for thermal aware analysis of OR-XNOR based network synthesis using dual Reed-Muller (RM) expansion. RM expressions are preferred over other forms of expansions because of higher testability rate [10] and lower switching signals [11]. At logic level, the value of temperature is unknown; however, it can be controlled by limiting the power-density [12] as depicted in equation 1.

$$Temp_{chip} = Temp_{amb} + R_{th}\left[\frac{Total_{Power}}{Total_{Area}}\right] \quad (1)$$

Here, '$Temp_{chip}$' and '$Temp_{amb}$' are the average chip temperature and ambient temperature respectively. 'R_{th}' is the summative equivalent thermal resistance of the substrate (Si) layer, package and heat sink. Total power dissipation and the total silicon chip area are represented by '$Total_{Power}$' and '$Total_{Area}$' respectively.

The rest of the paper is organized as follows: section II explains the background of MPDRM based circuit synthesis. Section III describes the tabular technique for polarity conversion and corresponding area, power and power density estimation. NSGA-II formulation for thermal-aware synthesis is described in section IV. Section V discusses the results obtained. Finally section VI draws the conclusion from the obtained result.

II. MIXED POLARITY REED-MULLER EXPANSIONS

An arbitrary multi input switching function $f(\tilde{x}_n, \tilde{x}_{n+1}, \ldots, \tilde{x}_1)$, can be represented as OR-AND based Canonical Product-Of-Sum (CPOS) form. The CPOS expansion with 2n different sum terms can be represented by equation 2:

$$f(\tilde{x}_n, \tilde{x}_{n+1}, \ldots, \tilde{x}_1) = \prod_{i=1}^{2^n}(q_i + \tilde{M}_i) \quad (2)$$

Here, $\prod$ represents the AND operator, $\tilde{M}_i$ is the max-term and qi $\epsilon\{1, 0\}$ indicates the absence or presence of max-terms respectively.

If each term in CPOS is expressed by all the variables of switching function then the AND term can be replaced by XNOR. This form of representation is called Dual Reed-Muller (DRM) expansion. A DRM expansion can be generalized by equation 3:

$$f(\tilde{x}_n, \tilde{x}_{n+1}, \ldots, \tilde{x}_1) = \Theta\prod_{i=1}^{2^n}(q_i + \tilde{M}_i) \quad (3)$$

If all the variables in equation 3 appear as true or complemented form at the same time, the expansion is known as Mixed Polarity Dual Reed-Muller expansion (MPDRM) [13-14].

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III. TABULAR TECHNIQUE FOR POLARITY CONVERSION

Polarity numbers are used to represent different MPDRM expansions. The polarity of each variable in MPDRM expansion are represented by ternary number 0, 1 or 2 depending on whether the variable is true, complementary or mixed. The representation of ternary number as MPDRM polarity is shown in equation 4.

$$< q_j >=< q_n, q_{n-1}, ... q_1 >$$

$$q_j = \begin{cases} 0 \;\; if \;\; \tilde{x}_k \;\; appears \;\; in \;\; true \;\; form \\ 1 \;\; if \;\; \tilde{x}_k \;\; appears \;\; in \;\; complemented \;\; form \\ 2 \;\; if \;\; \tilde{x}_k \;\; appears \;\; in \;\; mixed \;\; form \end{cases} \quad (4)$$

The parallel tabular technique for polarity conversion can be elaborated as follows:

i) The present and next state of polarities are represented by two sets of ternary operators as $q_p < q_n, q_{n-1}, ... q_1 >$ and $q_s < q_n, q_{n-1}, ... q_1 >$ respectively where, q_p and $q_s \in \{2, 1, 0\}$. Based on the polarity, three conditions may arise:

- Mixed form (q_p=2) to mixed form (q_s=2) conversion: In this type of conversion, the corresponding bit will be unchanged and no new term will be generated.
- Mixed form (q_p=2) to true form (q_s=0) conversion: When the present bit state is mixed form and need to convert into true form, the corresponding true forms will be unchanged but complementary state will be changed to true form with a new term consisting of don't care.
- Mixed form (q_p=2) to complementary form (q_s=1) conversion: In this case, all the complementary form of the variables are unchanged but true forms to be replaced by complementary and with a new term consisting of don't care will be added in the list.

ii) All the max-terms which define the switching function are listed in the index table and the counting index of all the max-terms is set as 1.

iii) Select one of the max-term from the index table and generates all possible max-terms based on conversion technique discussed in step (i).

iv) If the newly generated term is already in the index table, increment the index count by 1. Otherwise, add it to the index table and set the number of index count to 1.

v) Same procedure from step (i) to (iv) is followed for all the max-terms listed in the index table.

vi) The terms with even index numbers are eliminated and the terms with odd index number represent the switching function with desired polarity.

A. Area Estimation of MPDRM Network

When a combinational circuit is decomposed into MPDRM expansion then total number of max-term can be accounted as representative area.

B. Power Estimation of MPDRM Network

Dynamic power consumption of MPDRM circuit is considered here for the estimation of the power consumption. Dynamic power consumption occurs mainly because of charging and discharging of nodes and load capacitances. It is given by equation 5.

$$p_{dynamic} = \alpha_L C_L V_{DD}^2 f + \sum_i \alpha_i C_i V_{DD} (V_{DD} - V_T) f \quad (5)$$

Here, 'α_L' and 'α_i' are the switching activity at the load and internal node respectively. 'C_L' and 'C_i' are the load and internal capacitance respectively. 'V_{DD}', 'V_T' and 'f' indicate the supply voltage, threshold voltage and frequency of operation respectively. Other than switching activity, all parameters are user or manufacturer defined. Keeping all these constants, dynamic power consumption can be controlled by controlling switching activity. Hence, switching activity is considered as power metric at the logic level.

Let us consider that initial inputs are uncorrelated and statically independent of each other, that is, $Prob_{(input = 0)} = Prob_{(input = 1)} = 0.5$. If the present state of the output changes its previous state then only output of a logic gate changes its state. Thus, the probability of the output of a gate changing its state is $Prob_{(present\_output = 0)}$ X $Prob_{(previous\_output = 1)}$ + $Prob_{(present\_output=1)}$ X $Prob_{(previous\_output=0)}$. Here, we have considered that the probability does not change with time, then the switching activity of a logic gate can be expressed as to 2 X $Prob_{(output=0)}$ X $Prob_{(output=1)}$. Switching activity for '*i*' variable sum term is given by:

$$\alpha_{OR} = 2 \text{ X } \left(\frac{1}{2^i}\right) \text{ X } \left[1 - \left(\frac{1}{2^i}\right)\right] \quad (6)$$

Computation of switching activity for XNOR gate with 'j' inputs function with 'k' ON probability can be expressed as:

$$\alpha_{XOR} = 2 \text{ X } \left(\frac{k}{2^i}\right) \text{X } \left[1 - \left(\frac{k}{2^i}\right)\right] \quad (7)$$

Summation of equation (6) and (7) provides the switching activity estimation of MPDRM expansion.

C. Power-Density Estimation of MPDRM Network

Power-density can be defined as the amount of power dissipated per unit area. It can be defined by equation 8.

$$\text{Power} - \text{density}_{MPDRM} = \frac{\text{Power}_{MPDRM}}{\text{Area}_{MPDRM}} \quad (8)$$

The optimal solution lies in the large search space (3^n different polarities) of MPDRM expansions. The efficient polarity of MPDRM expansion can be achieved by a fast non-dominated sorting based meta-heuristic technique called NSGA-II.

IV. NSGA-II FOR THERMAL-AWARE SYNTHESIS

NSGA-II is a fast multi-objective algorithm with complexity $O(PQ^2)$, where P and Q represent the number of objective parameters and chromosomes in a population respectively [15-17]. A brief description of NSGA-II used for MPDRM problem formulation is given below.

A. Chromosome encoding

The '*n*' input variables $f=<x_1, x_2, x_3, ..., x_n>$ represent with polarity $p_x=<p_1, p_2, p_3, ..., p_n>$ where, polarities are either mixed, complemented and/or true based on ternary operator bit $p_x \in \{2, 1, 0\}$ as explained in equation 4. An example of six variable chromosome encoding is shown in Table I.

TABLE I. CHROMOSOME STRUCTURE

Variable	x_6	x_5	x_4	x_3	x_2	x_1
Polarity	0	1	2	1	0	2

B. Non-dominated sorting, front selection and rank assignment

Based on each objective function, the chromosomes are sorted into fronts based on non-domination count. The first front is assigned entirely to the non-dominant set of the current population. The subsequent front populations are

dominated by the chromosomes in the previous front only, and the front goes so on. Chromosomes in each front are assigned fitness concerning rank values or based on the front in which they exist. Different steps involved in non-dominated sorting are given below.

Step 1: Domination count (n[i]) of each chromosome is calculated by comparing with remaining chromosomes as:

If, ((area[i]>area[j]) || (Power[i]>Power[j]) || (Power_Density[i]> Power_Density [j]); then n[i] = 1.

Step 2: Front one is created by all chromosomes with n[i] = 1. The chromosomes those are dominated by front one are put in the front second and so on.

Step 3: Rank one is assigned to the chromosomes which are in the first front, and rank 2 is for the second front chromosomes and so on.

C. Crowding distance

Crowding distance (i_d) enables the searching process by calculating Euclidian distance in the 'n' dimensional hyperspace for 'n' input variables to estimate the neighboring density of a solution in a population. Steps involved in crowding distance calculation are given below:

Step 1: Chromosomes are sorted in ascending order against each objective function and boundary solutions i.e., top (1) and bottom solutions (l) are assigned with infinite distance value ($i_d[1] = i_d[l] = \infty$). Other than boundary solutions, initial assignment of crowding distance are zero ($i_d[i] = 0$).

Step 2: Intermediate crowding distance is calculated against each objective function as:

$i_d[j] = i_d[j]+((i[j+1]-I[j-1])/(f_{max} - f_{min}))$

Here, 'f_{max}' and 'f_{min}' are the maximum and minimum objective function in a front respectively.

D. Parent selection

Parents are selected for crossover and mutation using tournament selection process based on the rank and crowding distance.

Step 1: Randomly two chromosomes are selected and their rank is examined. The chromosome having better rank is treated as a parent.

Step 2: If rank of both the chromosomes are same (belongs to same front), then their crowding distance is examined. The chromosome with better crowding distance is selected as a parent.

Step 3: Same procedure is followed to select another parent from the population.

E. Crossover

Two points crossover method is considered to generate 90% of 'N' chromosome by selecting two parents based on the parent selection procedure as mentioned. After selecting two parents, two random crossover points are selected and the polarities among the parent chromosomes are exchanged to form the child chromosome. Fig. 1 (a) and (b), explains the generation of two offspring chromosomes using crossover operation.

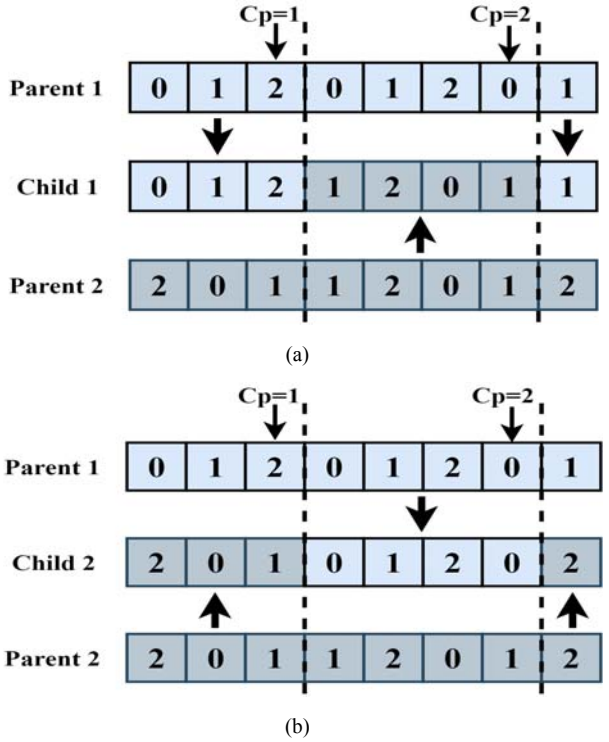

Figure 1. (a) Crossover operation method 1, (b) Crossover operation method 2

F. Mutation

Mutation operation is performed by selecting few random bit positions called mutation points (mp) and the polarity of those selected positions are altered by roulette wheel criteria as shown in Fig. 2 (b). The three positions of the wheel contain the polarity number. A random number is generated within 0 to 1 for each mutation point. The wheel moves clockwise if the generated random number is greater or equal to 0.5, otherwise anti-clockwise. 10% of 'N' chromosomes are generated using mutation operation. Fig. 2 (a) shows the method of offspring generation using mutation operation.

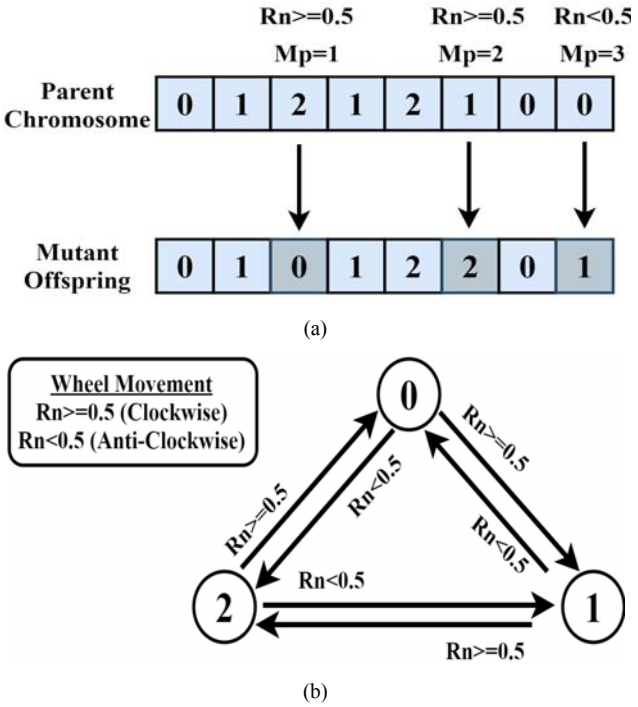

Figure 2. (a) Mutation operation; (b) Roulette wheel criteria

The selected parent chromosomes generate 'N' offspring chromosomes using crossover and mutation operator. 'N' offspring combine with N parents to produce total population as '2N'. The best 'N' chromosomes from '2N' population are copied based on rank and crowding distance. Fig. 3 shows the process flow diagram of the proposed thermal-aware synthesis.

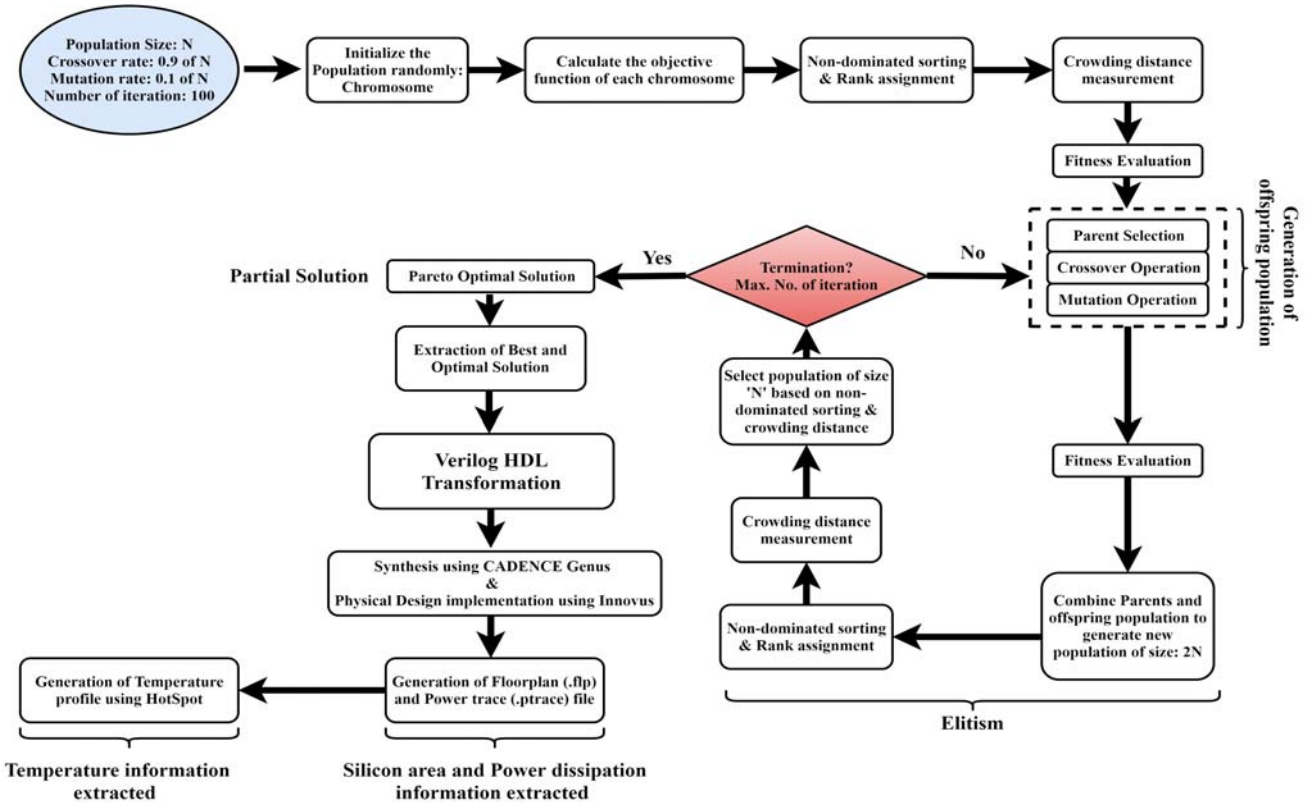

Figure 3. Process flow diagram of proposed thermal-aware synthesis

V. Results and Discussion

Proposed formulation for NSGA-II is enforced in LINUX based C-platform on a Pentium-IV machine with 3-GHz clock frequency and 4-GB RAM memory. MCNC benchmark suit is used for experimental validation. Chromosomes are encoded and decomposition of switching function based on polarities is done as explained in section IV-A. NSGA-II is employed to find efficient chromosome encoding based on area, power and power-density. 23 randomly chosen MCNC benchmark circuits [18] are tested for experimental validation. Table II gives the parameters and evolution operator's settings for proposed NSGA-II based approach. NSGA-II provides a Pareto optimal solution set consisting of best solutions and optimal solution considering all the objective parameters for each benchmark circuit. As an example case, Pareto optimal solution graph for 'lal' benchmark circuit is shown in Fig. 4. Area, power and power-density are represented by three axes of the graph. The solutions nearer to the origin represent the Pareto optimal front. Solutions nearer to each axis plain represent the best solution with respect to each objective function.

Table II. Parameters for Proposed NSGA-II Approach

Parameter	Value
No. of initial population	100.00
Total no. of iteration	200.00
Crossover probability	0.9
Mutation probability	0.1
Crossover operation	Two point crossover method
Mutation operation	Bit mutation based on Roulette wheel criteria
Termination criterion	Max. no. of iteration

Proposed approach is run 10 times on each circuit to reduce the impact of randomness on the results. Solutions obtained using NSGA-II based approach is considered as partial solution in terms of number of sum terms as area, switching activity as power and power density as temperature.

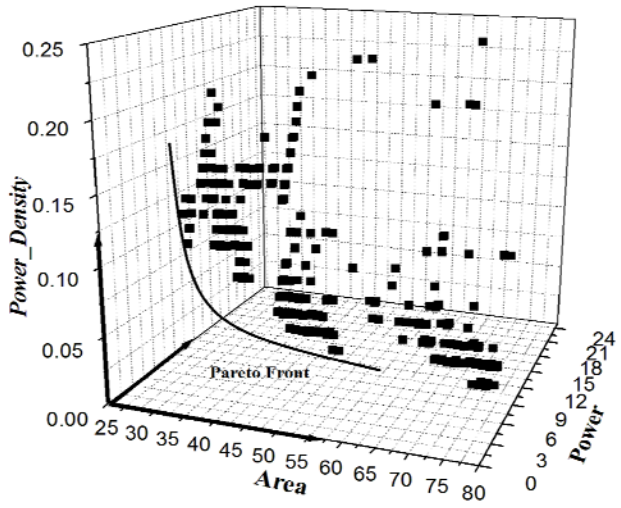

Figure 4. Pareto optimal graph of 'lal' benchmark circuit

To get the actual physical values of area in micrometer square, power in terms of nano-watts and temperature generation in degree centigrade, the optimum and best solutions obtained from NSGA-II are ported to verilog based hardware description language (HDL) for physical design implementation. Each benchmark circuit is implemented into physical design level using Cadence

Innovus digital design tool [19]. Taking synthesized netlist of the proposed circuit, Synopsis Design Constraints (SDC) library and Library Exchange Format (LEF) files at 45nm technology as inputs to the Innovus. Innovus generates the floorplan information (.flp) and power profile (.pptrace) containing the information of silicon area used and power dissipation. .flp and .pptrace files are further considered as input to HotSpot tool [20] to generate temperature profile for an individual circuit. Table III reports the comparative analysis of proposed approach with the Shared Reed-Muller Decision Diagram (SRMDD) based fixed polarity reed-muller network [7] and Shared Mixed Polarity Reed-Muller (SMPRM) network [8].

TABLE III. POST LAYOUT AREA, POWER AND TEMPERATURE ANALYSIS OF PROPOSED NSGA-II BASED APPROACH

Benchmark Circuits	Proposed MPDRM approach						SRMDD based approach [7]		SMPRM based approach [8]			CPU time (s)
	Best case			Optimum case			Best case		Best case			
	Area (μm^2)	Power (nW)	Temp (°C)	Area (μm^2)	Power (nW)	Temp (°C)	Area (μm^2)	Temp (°C)	Area (μm^2)	Power (nW)	Temp (°C)	
5xp1	17.78	206.67	67.81	36.25	443.87	69.30	559.88	76.70	140.22	1260.02	65.36	0.35
b12	12.92	77.42	61.90	19.99	140.28	63.18	-	-	-	-	-	0.38
clip	35.91	321.18	68.90	37.28	334.53	69.35	229.73	77.86	176.81	1358.89	68.20	0.37
cm162a	16.16	29.85	67.96	19.23	63.47	70.44	119.75	74.63	52.32	371.48	65.41	0.36
cm163a	14.45	31.52	66.80	14.45	39.82	69.30	169.65	73.98	35.91	187.69	63.05	0.35
cu	16.07	31.24	65.08	17.10	86.00	68.12	-	-	24.40	207.31	63.89	0.36
ex1010	126.54	1431.12	67.52	916.56	7433.37	69.81	-	-	-	-	-	0.63
inc	28.37	295.45	65.78	34.20	315.91	68.22	543.04	67.93	94.73	797.85	63.80	0.36
lal	14.02	42.43	62.04	34.20	104.71	62.29	758.42	97.53	-	-	-	0.36
misex1	40.69	462.38	65.39	41.04	543.24	66.57	239.71	73.02	39.67	303.06	63.54	0.35
misex2	47.54	400.08	66.94	76.19	400.08	67.18	-	-	49.68	354.40	63.20	0.35
misex3	267.10	3054.74	68.62	459.30	5456.12	70.19	-	-	290.21	1557.40	66.50	0.45
pcler8	16.16	49.83	60.96	18.21	68.40	60.96	606.24	67.93	-	-	-	0.36
pm1	10.26	74.58	62.29	12.65	115.18	64.49	-	-	15.09	182.05	62.33	0.35
rd53	13.42	26.23	68.14	13.42	42.17	70.98	149.87	84.90	21.02	328.58	65.92	0.35
rd73	13.07	23.25	69.69	13.42	34.69	71.21	446.57	78.41	40.96	598.21	68.96	0.36
rd84	17.86	78.43	69.41	21.97	126.18	70.86	-	-	57.45	731.74	68.71	0.35
sao2	22.91	201.13	68.40	22.91	201.13	70.48	-	-	96.30	963.07	65.48	0.37
sct	15.39	137.54	66.30	17.78	170.66	67.18	-	-	-	-	-	0.36
table3	189.77	2628.25	67.28	538.31	3866.28	69.72	-	-	728.12	2343.71	66.07	0.67
table5	215.67	261.73	65.34	638.74	526.16	66.31	-	-	-	-	-	0.70
ttt2	34.54	489.78	65.06	71.82	758.20	65.46	898.96	97.08	-	-	-	0.37
x2	12.65	179.46	64.83	17.78	205.48	65.35	166.53	96.57	27.70	170.46	62.27	0.35
Average % improvement of proposed approach w.r.t. SRMDD [7]	**92.43**	-	**16.56**	**90.93**	-	**14.82**						
Average % improvement of proposed approach w.r.t. SMPRM [8]	**51.21**	**44.97**	**-2.96**	**35.89**	**23.30**	**-5.70**						

It is observed from Table III that proposed best MPDRM solution saves 92.43% and 51.21% area with respect to SRMDD and SMPRM based solution. When the proposed optimum solution is considered, the proposed work shows an improvement of 90.93% and 35.89% area with respect to SRMDD and SMPRM based solution. When power solutions are compared, the proposed best solution shows 44.97% and optimum solution shows 23.30% power savings with respect to SMPRM based solutions. Proposed work shows a temperature savings of 16.56% and 14.82% with respect to SRMDD based solution for best case and optimum case respectively. But in case of SMPRM, the proposed work shows an overhead of 2.96% for best case and 5.70% for proposed optimum case. The average percentage improvement of proposed work with respect to fixed polarity based SRMDD and mixed polarity based SMPRM are shown in Fig. 5 and 6 respectively. The last column reports the maximum CPU time in seconds required to implement the circuits in an identical cadence Innovus platform.

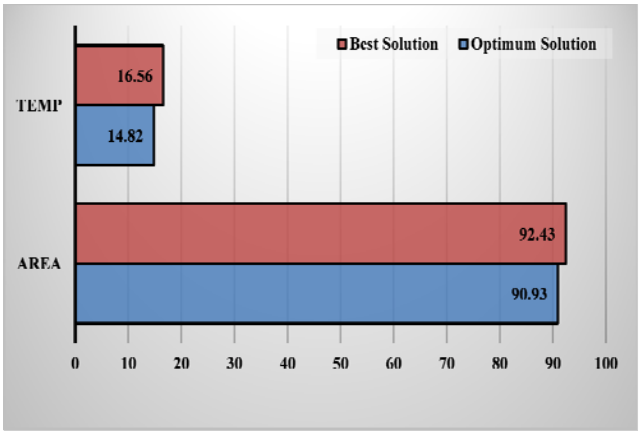

Figure 5. Average percentage improvement of proposed approach with respect to fixed polarity based SRMDD based network.

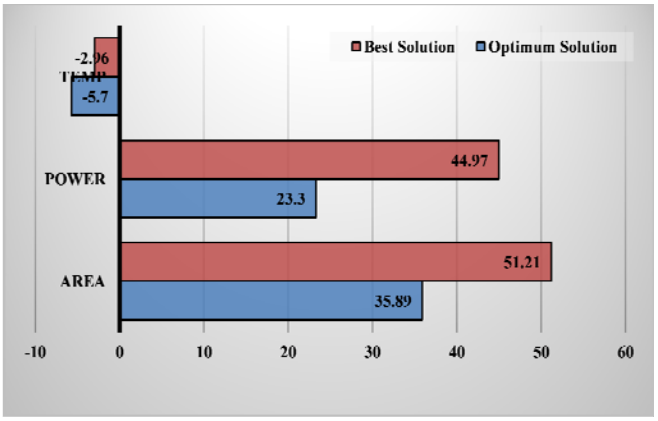

Figure 6. Average percentage improvement of proposed approach with respect to fixed polarity based SRMDD based network.

VI. Conclusion

In this work, we proposed a non-dominated sorting genetic algorithm-II based parallel tabular technique to find the optimal input variable polarity for mixed polarity dual reed-muller network for the area, power, and temperature optimization. The performance of the proposed approach is validated using the MCNC benchmark suit. The major findings of the proposed work can be summarized as follows:

- NSGA-II is applied as a heuristic algorithm to find the optimal mixed polarity in MPDRM network.
- Input variable polarity conversion is done using a parallel tabular technique.
- A Pareto optimal solution set is reported consisting of the best solution of each objective function and optimum solution considering all parameters.
- The proposed algorithm for MPDRM is compared with fixed polarity based SRMDD based network and mixed polarity based SMPRM based network.
- Physical design implementation using CADENCE Innovus tool is done to obtain the actual silicon area in micrometer square and power report in nano-watt.
- Absolute temperature at degree centigrade is generated for each design modeled using HotSpot tool.
- Significant improvement in area and power is observed with respect to fixed and mixed polarity based reed-muller network.
- When the peak temperature is compared, it is observed that the proposed MPDRM network shows a reduction of around 16.56% peak temperature with respect to SRMDD based network but shows an overhead of around 2.96% when compared with the SMPRM based network.

References

[1] L. Shang and R. P. Dick, Thermal crisis: challenges and potential solutions. IEEE Potential, vol. 25, pp. 31-35, 2006. doi: 10.1109/MP.2006.1692283

[2] A. Das, A. Debnath & S N Pradhan, "Area, power and temperature optimization during binary decision diagram based circuit synthesis," in Proc. IEEE Devices for Integrated Circuit, 2017, pp. 778-782. doi: 10.1109/DEVIC.2017.8074058

[3] A. Iranfar, M. Kamal, A. Afzali-Kusha, M. Pedram & D. Atienza, "Thespot: Thermal stress-aware power and temperature management for multiprocessor systems-on-chip," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 37, no. 8, pp. 1532-1545, 2018. doi: 10.1109/TCAD.2017.2768417

[4] W. L. Hung, Y. Xie, N. Vijaykrishnan, C. Addo-Quaye, T. Theocharides & M. J. Irwin, "Thermal-aware floorplanning using genetic algorithms," in Proc. IEEE 6th international symposium on quality electronic design (isqed'05), 2005, pp. 634-639. doi: 10.1109/ISQED.2005.122

[5] S. H. Gunther, "Managing the impact of increasing microprocessor power consumption," Intel Technology Journal, vol. 5, no. 1, pp. 1-9, 2001.

[6] A. Das & S. N. Pradhan, "Thermal aware FPRM based AND-XOR network synthesis of logic circuits," in Proc. IEEE 2nd International Conf. on Recent Trends in Information Systems (ReTIS), pp. 497-502, 2015. doi: 10.1109/ReTIS.2015.7232930

[7] A. Das & S. N. Pradhan, "Shared Reed-Muller decision diagram based thermal-aware AND-XOR decomposition of logic circuits," VLSI Design, vol. 2016, pp. 1-14, 2016. doi: http://dx.doi.org/10.1155/2016/3191286

[8] A. Das & S. N. Pradhan, "Area-Power-Temperature Aware AND-XOR Network Synthesis based on Shared Mixed Polarity Reed-Muller Expansion," International Journal of Intelligent Systems and Applications, vol. 10, no. 12, pp. 35-46, 2018. doi: 10.5815/ijisa.2018.12.04

[9] A. Das & S. N. Pradhan, "Thermal-aware Output Polarity Selection Based on And-Inverter Graph Manipulation," Recent Advances in Electrical & Electronic Engineering, vol. 12, no. 1, pp. 30-39, 2019. doi: https://doi.org/10.2174/2352096511666180320120016

[10] N. Alon, T. Kaufman, M. Krivelevich, S. Litsyn, & D. Ron, "Testing reed-muller codes," IEEE Trans. on Inf. Theory, vol. 51, no. 11, pp. 4032-4039, 2005. doi: 10.1109/TIT.2005.856958

[11] P. Wang, J. Lu, J. Xu, & J. Dai, "Power optimization algorithm based on XNOR/OR logic," Journal of Electronics, vol. 26, no. 1, pp. 138-144, 2009. doi: 10.1007/s11767-007-0064-6

[12] M. Pedram & S. Nazarian, "Thermal modeling, analysis, and management in VLSI circuits: Principles and methods," in Proc. of the IEEE, vol. 94, no. 8, pp. 1487-1501, 2006. doi: 10.1109/JPROC.2006.879797

[13] M. Yang, L. L. Wang, J. R. Tong & A. E. A. Almaini, "Techniques for dual forms of Reed–Muller expansion conversion," Integration, vol. 41, no. 1, pp. 113-122, 2008. doi: https://doi.org/10.1016/j.vlsi.2007.02.001

[14] Y. Haizhen, J. Zhidi, W. Pengjun, & L. Kangping, "GA-DTPSO algorithm and its application in area optimization of mixed polarity XNOR/OR circuits," Journal of Computer-Aided Design & Computer Graphics, vol. 27, no. 5, pp. 946-952, 2015.

[15] K. Deb, A. Pratap, S. Agarwal & T. A. M. T. Meyarivan, "A fast and elitist multiobjective genetic algorithm: NSGA-II," IEEE trans. on evolutionary computation, vol. 6, no. 2, pp. 182-197, 2002. doi: 10.1109/4235.996017

[16] K. Deb, "Multi-objective optimization using evolutionary algorithms," John Wiley and Sons, 2003.

[17] D. S. H. Ram, M. C. Bhuvaneswari & S. Umadevi, "Improved low power FPGA binding of datapaths from data flow graphs with NSGA II-based schedule selection," Advances in Electrical and Computer Engineering, vol. 13, no. 4, pp. 85-92, 2013. doi: 10.4316/AECE.2013.04015

[18] MCNC benchmark suit, http://ddd.fit.cvut.cz/prj/Benchmarks/

[19] Cadence Innovus implementation system, https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/innovus-implementation-system-ds.pdf.

[20] HotSpot, http://lava.cs.virginia.edu/HotSpot/