Phase-Locked Loop with Inverse Tangent based Phase Detection

Djordje STOJIC
Electrical institute Nikola Tesla, Koste Glavinica 8a, 11000 Belgrade, Serbia
djordje.stojic@ieent.org

***Abstract*—In this paper, a novel closed-loop synchronization algorithm is proposed based on the linear phase angle detection. The linear phase detection is performed by the inverse tangent (atan2) trigonometric function, while the frequency tracking is performed by a proportional-integral (PI) loop filter and phase integrator. By using the linear phase detection, the linear phase-locked loop (PLL) is employed, which is simpler to implement and to tune, and which also performs better for large frequency and phase variations when compared to conventional PLL algorithms. Also, the novel technique operates consistently for a whole range of designated PLL crossover frequencies when compared to existing PLL techniques, which makes it a better candidate when higher filtering is required of higher harmonics and measurement noise. When compared with existing algorithms that use atan function for phase angle estimation, the novel algorithm enables the frequency estimation that does not include differentiation, which improves the resulting algorithm immunity to measurement noise and higher harmonics. The novel PLL is tested by simulation and experimental runs.**

***Index Terms*—estimation, frequency locked loops, nonlinear control systems, phase locked loops, power conversion.**

I. INTRODUCTION

Synchronization of power converters with the grid voltage represents an important task in a wide range of applications. From the grid-tied AC and DC power converters [1-6], distributed power generation utilities [7-9], to AC motor drives [10], synchronization comprises the input AC signal frequency and phase angle estimation, which need to be fast and robust in relation to the input signal disturbances. There is a wide range of different synchronization techniques, which can be divided into two major groups–open and closed-loop [3]. In the closed-loop methods, the input signal frequency and phase angle are estimated by a feedback-loop mechanism. The closed-loop concept (i.e. the phase-locked loop) is considered to be more frequently employed in the power converter design.

The primary task of an efficient synchronization algorithm is to resolve two opposing requirements–the synchronization response time should be fast, while it, also, needs to be robust in relation to the disturbances, harmonics and noise present in the input signal. In [4], major requirements for synchronization algorithms are outlined in different power converter applications. They include the synchronization operation contaminated by the measurement noise and harmonics, including the unbalanced base signals. The operation of the synchronization with the variable base signal frequency is also assumed. In [7], the grid code requirements are outlined, defined for the distributed power generation applications, which are mainly concerned with the photo-voltaic and wind-based power generation system performances in low-voltage-ride-through operation.

In [3] and [7], an analysis is presented based on the hypothesis that the closed-loop synchronization techniques provide more robust solutions in relation to the base signal disturbances. However, in [11] it is shown that commonly used PLL solutions (based, for example, on dqPLL [7], [11], [13], power-PLL [2], or EPLL algorithms [4], [12]) all rely on a nonlinear phase detection (PD). This influences the PLL dynamic performance for large frequency and phase variations, and, also, its sensitivity in relation to base signal disturbances. In [1] and [11] the PLL parameter tuning procedures are presented based on the PD linearized transfer function, derived for small-signal variations around the base frequency and phase values. Consequently, the corresponding dynamic analysis is predominantly valid for the narrow band around the base frequency values, while a different PLL dynamic performance should be expected for wider frequency and phase deviations. This becomes especially significant in the cases of the PLL that includes additional phase error filtering to reduce the PLL sensitivity in relation to higher harmonics and disturbances present in the input PLL signal.

In this paper, the novel PLL is proposed based on the atan2 function phase detection. In this way, feedback-loop synchronization is realized based on the phase detection that has a linear model in a whole phase angle range, so a linear PLL loop-filter design can be employed that guarantees the same level of dynamic performance for all operating conditions. Because of its linear model, the novel PLL has better transient performance for large phase angle and frequency changes when compared with dqPLL, power-PLL, and EPLL applications. When compared with existing PLL techniques based on atan function phase angle estimation, the novel technique enables frequency estimation that does not require differentiation, thus increasing the immunity to measurement noise. Also, in the new PLL additional filtering can be employed in an easier manner since it operates effectively in a whole range of designated PLL crossover frequencies, which may be required in order to reduce the influence of the higher harmonics and disturbances.

Finally, when compared to dqPLL, power-PLL and EPLL, the novel atanPLL is easier to implement on a digital control platform, which is illustrated in the Section 5.

Consequently, the main contribution introduced in this paper is related to the solutions [9], [25-27] and [29]. When compared with [9], [25-26] open-loop atan function based PLLs, a novel solution enables the input signal frequency

This work was supported by Ministry of Science in Serbia.

Digital Object Identifier 10.4316/AECE.2021.01004

estimation with no differentiation used, which would amplify the noise and higher harmonic components in the input signal. When compared with [27] simpler solution is used, less prone regarding higher harmonic content. Regarding the closed-loop algorithm [29], which is the most similar to the new solution, more detailed estimated frequency prewarping function is proposed, combined with a simpler solution that does not require any additional rotational transformations.

This paper comprises six sections. In Section 2 the existing synchronization techniques are presented, while in Section 3 the novel atanPLL method is proposed. In Section 4 the set of simulation runs is presented, in order to illustrate the improvements introduced by atanPLL when compared to conventional dqPLL. Section 5 includes experimental results, in order to verify the speed and robustness of novel PLL.

II. Literature Review

In this section, several major synchronization techniques are outlined, which may be divided into two groups–open and closed-loop. In open-loop algorithms, the phase angle is usually calculated in the $\alpha\beta$ reference frame, based on filtered samples of input signals. In closed-loop algorithms, the phase angle value is locked by a feedback-loop mechanism.

A. Open-loop synchronization

In this paper, four basic open-loop synchronization techniques are outlined.

1) Zero-crossing method

The zero-crossing method represents the simplest variant of synchronization, which is highly sensitive in relation to the harmonics and disturbance components in the input signal. Also, the synchronization time depends on the frequency of the input signal [9].

2) Filtered grid-voltages based open-loop synchronization

To improve the zero-crossing method, the open-loop synchronization techniques are proposed based on filtering the input signal. In [9] two basic approaches are outlined–low-pass filter implemented in the rotating dq reference frame, and a band-pass filter in the stationary $\alpha\beta$ reference frame. In both cases, the synchronization is performed by the atan function. However, in the stationary frame based method additional filter lag compensation is required in order to get accurate synchronization. Although, compared to the zero-crossing filtered approach this improves the operation, it is still sensitive in relation to harmonics and disturbances. In the new solution, atan based phase detection is employed in the closed-loop synchronization algorithm, which makes frequency detection less prone regarding input noise and higher harmonics.

3) State-space model based techniques

The voltage amplitude, frequency, and phase can be estimated by various state-space model based techniques. They include extended Kalman filter (EKF) [15], space vector filter (SVF) [16], and weighted least-squares estimation (WLSE) [17] based methods. With EKF, if the grid voltage model is provided the phase value can be successfully estimated. However, this method does not operate for the unbalanced grid voltage conditions, and the EKF calculation time is relatively long. The SVF represents an effective tool for the input grid voltage vector low-pass filtering, which is sensitive in relation to the grid voltage frequency variations. Finally, while the WLSE successfully solves the EKF and SVF problems related to their accuracy under unbalanced input conditions and frequency variations, it exhibits high computation requirements related to the least-squares method calculation.

4) Discrete Fourier transform (DFT) filtering based open-loop synchronization

In [3], the open-loop synchronization technique based on DFT filtering is proposed. This method uses DFT to estimate the phase angle value, enabling the one cycle estimation transient response. Also, DFT is combined with existing frequency estimation techniques, in order to provide an universal synchronization technique that is immune to harmonics and disturbances in the input signal. A technique based on a generalized approach for computing all, or a part of DFT, known as Chirp-Z transform (CZT) is proposed in [23]. The major difference between CZT and DFT, is that CZT can improve spectral resolution and measurement accuracy around the power supply frequency. However, the shortcoming of these methods is their high computational demand.

In [28], a modification of DFT based open-loop synchronization algorithm is proposed, which includes a low-pass notch (LPN) filter instead of the DFT based signal filtering used to determine the input signal components used for the phase angle estimation by implementing the atan function. Though the LPN bases open-loop synchronization is simpler to implement than DFT [3], it still requires independent frequency estimation, which makes it more complex when compared to the novel atanPLL solution.

5) Additional open-loop synchronization techniques based on atan function phase angle estimation

In [25-27], additional open-loop synchronization techniques are proposed, which use atan function to estimate the input signal phase angle value. Solutions [25, 26], contrary to the new atanPLL, use differentiation to estimate the input signal angular frequency value, which makes them more prone to the measurement noise and higher harmonics. In [27], a different algorithm is employed for the frequency estimation based on the inverse trigonometric calculus, which is more complex when compared with the novel atanPLL. In the new solution, the sensitivity in relation to the measurement noise is reduced by omitting the differentiation in the input signal frequency estimation, while the sensitivity of [27] regarding the higher harmonics improved by introducing linear atan based phase angle, and closed-loop PLL based frequency estimation.

B. Closed-loop synchronization

The closed-loop synchronization techniques (i.e., PLL) are based on a feedback structure in which the estimated phase angle error is regulated to the zero value [4]. The basic outline of a closed-loop synchronization algorithm comprises three elements – the phase detector (PD), the loop filter (LF), and the voltage-controlled oscillator (VCO).

Commonly, PLL operates with a three-phase input signal–however, there are also single-phase PLL variants [1], [6]. In PLL, the phase estimation response time is

$$\theta_{est}(k)=\begin{cases}\theta_{est}(k)=\theta_{est}(k-1)+T_s y_{lf}(k)-2\pi, & \text{for } \theta_{est}(k-1)+T_s y_{lf}(k)>\pi\\ \theta_{est}(k)=\theta_{est}(k-1)+T_s y_{lf}(k), & \text{for } \theta_{est}(k)+T_s y_{lf}(k)\in[-\pi,\pi]\\ \theta_{est}(k)=\theta_{est}(k-1)+T_s y_{lf}(k)+2\pi, & \text{for } \theta_{est}(k-1)+T_s y_{lf}(k)<-\pi\end{cases} \quad (1)$$

determined by the PD and LF, where LF can also be designed regarding the required level of rejection of the disturbance and harmonics. The following are the three major PLL techniques, which are conventionally used for the synchronization of power converters to the power grid.

1) The synchronous frame based dqPLL

The synchronous frame based dqPLL in Fig. 1 represents one of the more commonly used synchronization techniques, where ω_{ff} represents the feed-forward estimated frequency value (usually equal to 2π50 rad/s or 2π60 rad/s).

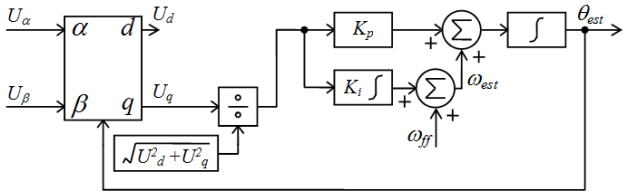

Figure 1. The synchronous frame based dqPLL

Here, the PD is implemented by a *dq* rotational transformation, synchronous with the input signal in the stationary state. The LF is implemented by a proportional-integral (PI) controller, used to regulate the estimated frequency value in order to drive the U_q component to zero, and also to filter the noise and harmonics present in the input PLL signal. The phase angle value is estimated by an integrator. The outlined U_q signal normalization is required in order to get the same PLL dynamics for different input signal amplitude values.

The PI controller parameters are tuned according to two opposing requirements, which require a certain level of trade-off: fast phase tracking and good filtering. Since the PD used represents a nonlinear element, the PI is tuned by linearization, by approximating $\sin(\theta^*-\theta_{est})$ with $(\theta^*-\theta_{est})$, where θ^* represents the phase angle of the input signal $U_{\alpha\beta}$, and θ_{est} the estimated phase angle value. Also, in Fig. 1 ω_{est} represents the estimated frequency value. The most commonly used PI controller parameter tuning procedure is the symmetrical optimum method, which is used in [1,4,11,18]. In this paper, extended symmetrical optimum method is employed, which is proposed in [30] and employed in [31].

2) Extended PLL

The extended PLL [4,12] also represents the closed-loop synchronization technique based on a nonlinear PD, as in dqPLL. However, it originally operates in single-phase synchronization applications, since it provides a π/2 shifted input signal component required for the synchronization.

3) DFT PLL

The DFT PLL [14,18-20] is outlined in following Fig. 2, since it represents one of the currently existing methods that incorporates the atan function based closed-loop phase angle synchronization, similar to the novel PLL proposed in this paper.

In this method, the DFT component calculation is performed at the nominal input signal frequency, by a corresponding sine and cosine factorization and moving average filtration (MAF), where the MAF window is equal to the period of the base input signal. The phase angle is calculated by performing the atan function on the calculated DFT components at the base frequency. Although this method has high immunity regarding the measurement noise and input signal harmonic contamination, it is sensitive in relation to the input signal frequency variations, i.e., it exhibits a high double frequency error for high grid frequency deviations. Also, for the variable input frequency variations, it is difficult to implement the corresponding adaptive MAF.

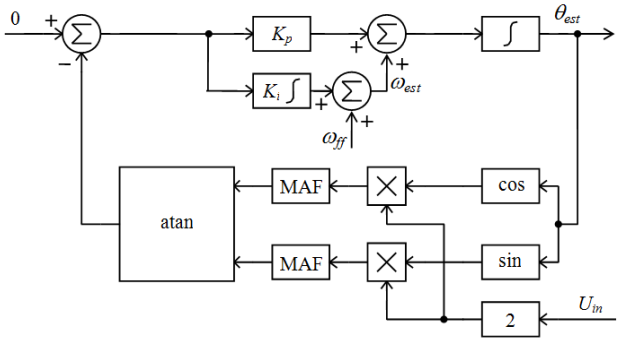

Figure 2. The atan function based DFT PLL

4) Additional closed-loop synchronization techniques based on atan function phase angle estimation

In [29] Quasi Type 1 PLL is presented in which the atan function is, similarly as in new atanPLL, used for the phase angle estimation in combination with the closed-loop frequency estimation. However, in [29] problem of the phase angle prewarping is not addressed, which is necessary if closed-loop frequency estimation needs to be implemented. Also, in [29] additional rotational transformations are required, which is not the case in the new atanPLL. The higher harmonics filtration, which is implemented in [29] by a moving average filter or a low-pass filter (LPF), can in the atanPLL case, also, successfully be implemented by LPFs realized in $\alpha\beta$ stationary reference frame. Consequently, the main contribution of the new solution regarding [29] comprises the designated frequency prewarping algorithm and a simpler structure that does not include additional rotational transformations.

In Section 3 the novel atanPLL is proposed.

III. New Atan2 Function Based PLL

In Fig. 3, the PLL method is presented based on the feedback-loop estimation of the input signal frequency and phase angle values, with the atan2 function based PLL input.

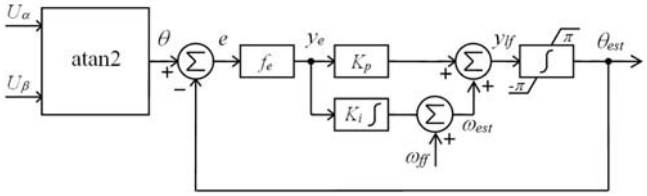

Figure 3. The novel atanPLL

Since the atan2 function output θ in Fig. 3 (for the input signal $U_{\alpha\beta}$ with the constant frequency ω) represents a discontinuous signal varying in the range [-π, π], the integrator used to estimate the phase value θ_{est} (integrator θ in Fig. 3) needs to be changed accordingly (1), where $y_{lf}(k)$ represents the LF output signal.

This is done in order to get the continuous frequency estimation ω_{est} that is not influenced by discontinuities in the atan2 function output, where T_s in (1) represents a sampling period. To get the continuous ω_{est} estimation for the discontinuous atan2 function output, the function f_e (2) is introduced in Fig. 5. In this way the prewarping function of the estimated frequency value is obtained. Both the dqPLL in Fig. 3 and atanPLL in Fig. 5 can be modelled by the open-loop transfer function $W(s)$ (3) and closed-loop transfer function $G_{PLL}(s)$ (4), where T_s represents a sampling period, e the estimated angle error, and K_p proportional and K_i integral LF gains.

$$f_e(e)=\begin{cases} e-2\pi, & e>\pi \\ e, & \text{for } e\in[-\pi,\pi] \\ e+2\pi, & e<-\pi \end{cases} \tag{2}$$

$$W(s)=\left(K_p+K_i\frac{1}{s}\right)\frac{1}{s}\frac{1}{sT_s+1} \tag{3}$$

$$G_{PLL}(s)=\frac{\theta_{est}(s)}{\theta(s)}=\frac{W(s)}{1+W(s)} \tag{4}$$

One of the main advantages of the proposed atanPLL algorithm, when compared to the conventional PLL methods, is that for the novel estimator the open-loop (3) and closed-loop (4) transfer functions are linear for all operating conditions (i.e., for both small and large input signal frequency and phase variations). This is contrary to, for example, dqPLL and DFT PLL solutions, which, because of the nonlinear PD nature, exhibit linear performance only for smaller phase and frequency variations [24].

Regarding the open-loop estimators, the primary advantages introduced by the novel PLL are:

- the atanPLL enables input signal frequency estimation, which is important in single-phase [1, 6] and PLL applications with unbalanced input signals [21];
- the atanPLL enables simpler filtration of measurement noise and input signal harmonics by correspondingly tuning the LF PI controller parameters, without no phase lag compensation introduced by BPF in Fig. 1.

When compared to existing PLL applications, the following improvements are made:

- the atanPLL operates with PD linear for both small and large phase and frequency variations, contrary to dqPLL, DFT PLL, and EPPL, which significantly simplifies the LF PI controller parameter tuning and inclusion of additional filters in the synchronization loop;
- when compared to dqPLL, which requires four trigonometric functions, square root, and a division to be implemented, atanPLL requires one trigonometric function, which makes it much easier to implement and faster to run on any digital control equipment (in Section 5 it is shown that on a benchmark general purpose floating-point microcontroller atanPLL operates up to three times faster than dqPLL);
- because of linear PD features, the atanPLL behaves more consistently for large phase and frequency variations, when compared to conventional PLL applications [24], which is shown in the following sections 4 and 5;
- when compared to DFT PLL, the atanPLL enables easier operation with the variable input signal frequency values;
- the atanPLL enables simpler filtration of measurement noise and input signal harmonics by correspondingly tuning the LF PI controller parameters, since the proposed atan function based phase estimation enables the resulting PLL to operate consistently for a whole range of designated PLL crossover frequencies;
- when compared with open-loop synchronization techniques that use atan function to measure the input signal phase-angle value [25,26] the new atanPLL enables frequency estimation that is not based on differentiation, which causes amplification of measurement noise and higher harmonic in the input signals;
- when compared with [29] that also includes atan based phase estimation and closed-loop frequency estimation, the novel atanPLL introduces the phase angle prewarping function that is required to implement successfully the closed-loop frequency estimation. The atanPLL, also, does not require additional rotational transformations, which is a case in [29].

In the following subsection, the LF PI controller parameter tuning procedure is outlined.

A. PI loop filter parameter tuning procedure

The most commonly used PI loop filter parameter tuning technique is represented by the *symmetrical optimum method*, employed in [1], [4], [11], and [18]. In this paper, extended method is proposed, outlined in [30] and [31]. The primary goal of the *symmetrical optimum* LF filter parameter tuning method is to get the open-loop transfer function phase characteristic that is symmetrical around the chosen crossover frequency ω_c. This is achieved for the following set of LF parameter values [11]:

$$K_p=\omega_c \tag{5}$$

$$K_i=\omega_c^3 T_s \tag{6}$$

The setting of the designated crossover frequency ω_c is based on the objective that is related to the designated attenuation introduced by the loop filter at the double fundamental frequency component $2\omega_{ff}$. Consequently, the LF PI tuning is performed according to the chosen PLL crossover frequency ω_c, which is determined by the harmonic attenuation at $2\omega_{ff}$ introduced by the closed-loop PLL transfer function (4). In Fig. 4 the relation between the crossover frequency value ω_c and $G_{PLL}(s)$ (4) attenuation $Att_{@100Hz}$ at $2\omega_{ff} = 2\pi 100$ rad/s is presented, which is used to choose the ω_c value.

In this paper, two sets of LF parameters are calculated – for ω_{c1} that corresponds to $Att_{@100Hz}$ = -20 dB and for ω_{c2} that corresponds to $Att_{@100Hz}$ = -15 dB. This is done in order to illustrate the improvements introduced by atanPLL when

compared to dqPLL. For the chosen crossover frequency $\omega_c = \omega_{c1} = 64$ rad/s, and for the sampling period $T_s = 250$ μs, the PLL LF parameters are equal to $K_{p1} = 64$ and $K_{i1} = 65.5$, while for $\omega_c = \omega_{c2} = 114$ rad/s LF parameters $K_{p2} = 114$ and $K_{i2} = 370$ are got.

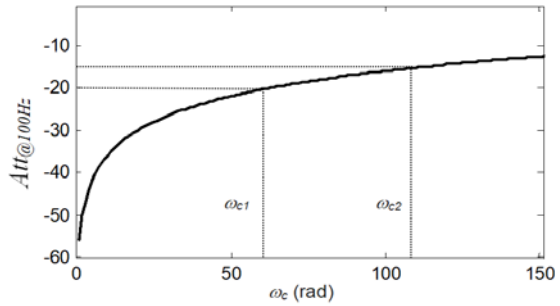

Figure 4. Relation between PLL crossover frequency ω_c and attenuation at 100 Hz $Att_{@100Hz}$

IV. Simulation Results

In Section 4 the results of the simulation tests are compared for dqPLL and atanPLL, operating in different conditions typical for the grid voltage synchronization, for the previously calculated sets of LF parameters. For the set of PLL LF parameters determined in the previous section, the following two sets of simulations are performed, for dqPLL and atanPLL – (i) phase angle jump, and (ii) frequency jump. It is shown that novel atanPLL outperforms the conventional dqPLL for large frequency and phase angle jumps, because of the linear nature of the PD used in atanPLL contrary to the nonlinear PD used in dqPLL. The simulation runs are performed for PLLs with two different sets of LF parameters, designed for crossover frequency values $\omega_c = 64$ rad/s and $\omega_c = 144$ rad/s in Section 3.

A. Phase jump test

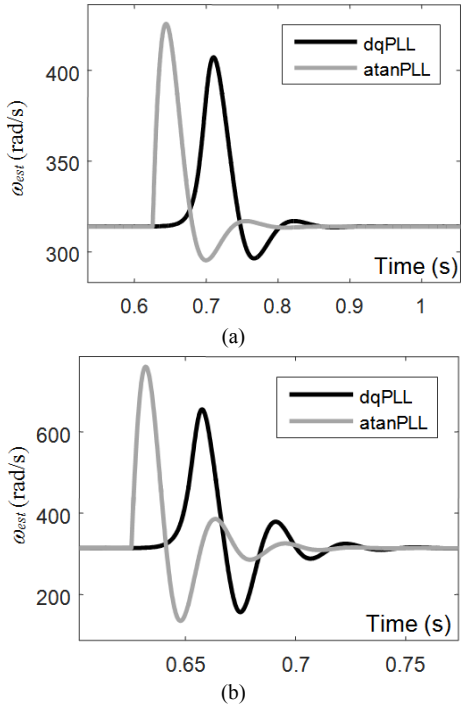

Figure 5. The $\Delta\varphi = \pi$ rad phase jump for dqPLL and atanPLL, for $\omega_{ff} = 2\pi 50$ rad/s, (a) $\omega_c = 64$ rad/s and, (b) $\omega_c = 114$ rad/s

In this subsection the simulation results are presented for two different PLL algorithms – atanPLL and dqPLL – for the phase jump test. For the fundamental frequency $\omega_{ff} = 2\pi 50$ rad/s, phase angle jumps $\Delta\varphi = \pi$ rad are performed, for two different sets of LF parameters, resulting in the PLL responses outlined in Fig. 5.

By analyzing the simulation results in Fig. 5, it can be concluded that for both sets of LF parameters that correspond to ω_{c1} and ω_{c2}, the settling time t_{st} is with atanPLL (for (a) 150 ms and (b) 80 ms) faster than with dqPLL (for (a) 180 ms and (b) 100 ms). In this way, the improvement introduced by the novel atanPLL, compared to dqPLL, is directly illustrated, caused by the linear PD in atanPLL and nonlinear PD in dqPLL.

B. Frequency jump test

In the following subsection the simulation results are presented for the $2\pi 50$ rad/s frequency step jumps, presented in Fig. 6.

By analyzing the simulation results in Fig. 6(a) it can be concluded that, for $\Delta\omega = 2\pi 50$ rad/s, atanPLL has a rising time $t_r = 33$ ms that corresponds to the designated $\omega_c = 64$ rad/s (since $t_r \approx 2\pi 0.35/\omega_c$), while for dqPLL the large frequency jump caused a significant increase in the rising time value, with $t_r = 300$ ms. Similarly to the conclusions outlined in the previous subsection, this difference in the dqPLL and atanPLL performance can be explained by the nonlinear PD in dqPLL.

In Fig. 6(b), for both dqPLL and atanPLL, similar rising times are achieved ($t_r = 10$ ms), which leads to the conclusion that nonlinear dqPLL can perform similarly to linear atanPLL, for large frequency jumps, in the cases of the increased PLL cutoff frequency values. This means that atanPLL is more efficient than dqPLL when an increased filtration of the disturbances, harmonics and measurement noise is required in PLL, which results in the need to operate with decreased PLL cutoff frequency values. The simulation test results are summarized in Table I, which is presented in the Appendix A.

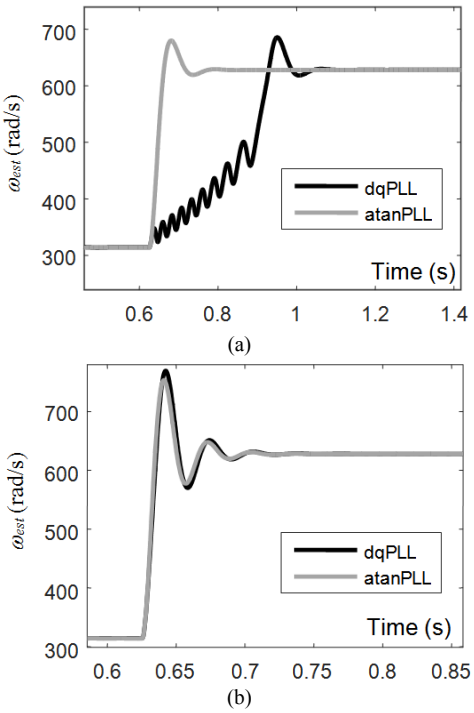

Figure 6. The 50 Hz frequency jump simulation test, for atanPLL and dqPLL, (a) $\omega_c = 64$ rad/s, (b) $\omega_c = 114$ rad/s

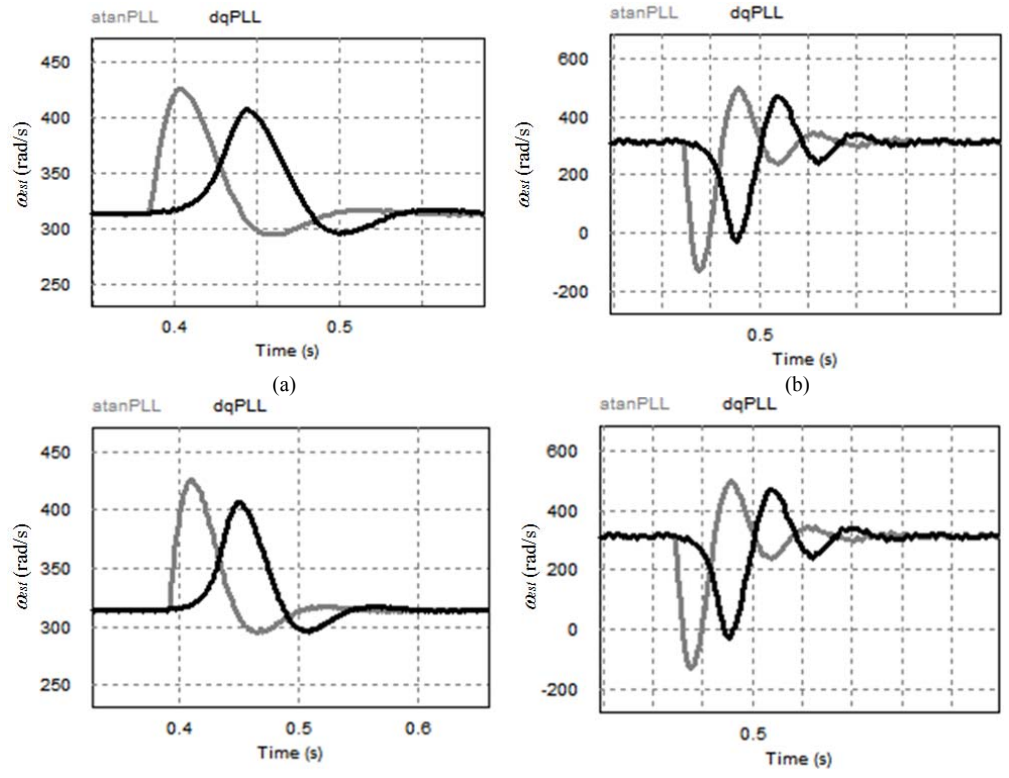

Figure 7. The $\Delta\varphi = \pi$ rad phase jump experimental results for, (a) $\omega_c =$ 64 rad/s and Test case 1, (b) $\omega_c = 114$ rad/s, Test case 1, (c) $\omega_c =$ 64 rad/s and Test case 2, and (d) $\omega_c = 114$ rad/s, Test case 2

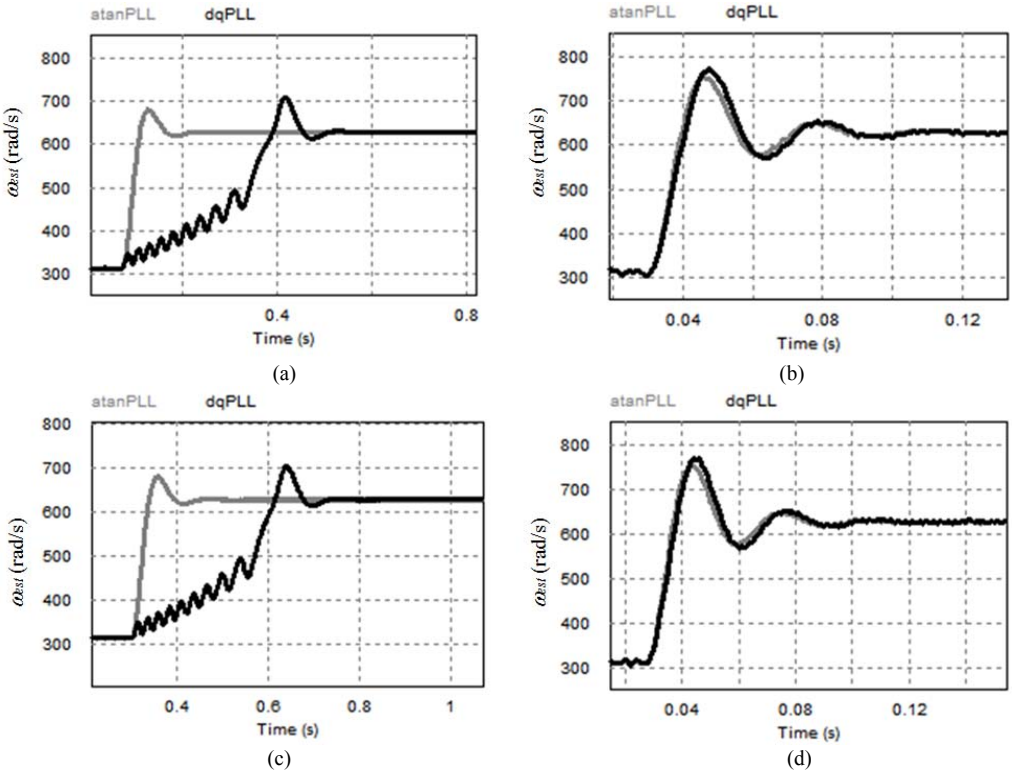

Figure 8. The $\Delta\omega = 2\pi 50$ rad/s frequency jump experimental results for (a) $\omega_c =$ 64 rad/s and *Test case 1*, (b) $\omega_c = 114$ rad/s, *Test case 1*, (c) $\omega_c =$ 64 rad/s and *Test case 2*, and (d) $\omega_c = 114$ rad/s, *Test case 2*

Similar conclusions regarding the significant increases in dqPLL response times for larger frequency jumps are, also, made in [24]. However, it is shown that atanPLL can solve this problem successfully.

V. Experimental Results

In this section the atanPLL and dqPLL performances are examined by implementing these algorithms by the control card based on the floating-point digital signal processor (DSP) TMS320F28335, with the sampling period $T_s = 250$ µs. For the case of benchmark TMS320F28335 DSP the atanPLL required 130 processor cycles, while dqPLL required 400 cycles to run, which illustrates the improvement introduced by atanPLL.

The experimental setup comprises the signal generator that produces α and β input PLL voltage components, with the harmonic content typical of the voltage grid signals [22].

Namely, two test sets of the used PLL input signals are defined in [22]:

Test case 1: $V_h = 1.0/2h$ pu for odd harmonics $h = -5, +7, -11, +13, -17, +19$, and $V_h = 1.0/2h/4$ for even harmonics $h = -2, 4, -8, 10, -14, 16, -20$, with the total harmonic distortion (THD) 16.0%;

Test case 2 for $V_h = 1.0/2h$ pu for $h = \pm5, \pm7, \pm11, \pm13$, with THD 27.3 %.

Two different cases of input PLL contaminated with higher harmonics are used in order to illustrate the difference between dqPLL and atanPLL performances when higher attenuation of harmonics and measurement noise is required. Namely, improvements that the novel atanPLL introduces when compared to conventional solutions can the most be illustrated in these cases when reduced PLL response speeds are required (for the higher level of noise and higher harmonics filtration, for example). These improvements are achieved because of the phase detection in atanPLL operates linearly in the entire range, while conventional solutions exhibit nonlinear phase detection for large input signal phase angle and frequency variations.

In the following subsections the results of two experimental tests, phase and frequency jumps, are presented, for two different PLL LF parameter values (designed for $\omega_c = 64$ rad/s and $\omega_c = 114$ rad/s), and for two different PLL input signals – *Test case 1* and *Test case 2*.

A. Phase jump test

In Fig. 7 the experimental results are presented for atanPLL and dqPLL designed for different crossover frequencies $\omega_c = 64$ rad/s and $\omega_c = 114$ rad/s, got for two sets of PLL input signals that contain different higher harmonics – *Test case 1* and *Test case 2*. To illustrate the improvements introduced by atanPLL when compared to conventional solutions, for aforementioned test cases large step changes equal to π are introduced. In this way, the advantage that atanPLL (with linear phase detection in whole operating range) has over conventional solutions (which operate with nonlinear phase detection for large phase angle variations) is emphasized.

After analysing the corresponding experimental results, following conclusions can be made. Regarding the estimated frequency ω_{est} response times similar conclusions can be made to those in subsection 4.1 – the atanPLL settling times are faster ($t_{st} = 150$ ms for $\omega_c = 64$ rad/s and $t_{st} = 80$ ms for $\omega_c = 114$ rad/s) compared to the dqPLL responses ($t_{st} = 190$ ms for $\omega_c = 64$ rad/s and $t_{st} = 95$ ms for $\omega_c = 114$ rad/s) – which can be attributed to the fact that atanPLL operates with the linear PD while dqPLL operates with the nonlinear PD.

Regarding the sensitivity in relation to harmonics, when analyzing the results in Fig. 7 (a) and (b) got for the Test case 1 PLL inputs it can be concluded that both atanPLL and dqPLL exhibit similar steady-state estimated frequency variations, which could be expected since both have similar disturbance attenuations. For the Test case 1, the ω_{est} variations for both atanPLL and dqPLL are $\delta = 1.2$ rad/s, while in Fig. 7 (b) they are equal to $\delta = 8$ rad/s. This increase in $\Delta\omega$ for the results in Fig. 7(b) when compared to Fig. 7(a) is caused by the fact that Fig. 7(b) contains results for PLLs designed for a smaller disturbance attenuation value at 100 Hz $Att_{@100Hz} = -15$ dB when compared to Fig. 10(a), which contains results got for PLLs designed for $Att_{@100Hz} = -20$ dB.

B. Frequency jump test

Similarly to experimental tests in subsection 5.1, in this subsection the tests are performed in which large step frequency jumps are introduced in the PLL input signals, to emphasize advantages of the linear phase detection in atanPLL when compared to nonlinear phase detection in conventional PLL solutions.

The results presented in Fig. 8 are like those in Fig. 6 regarding the differences in the frequency jump responses between atanPLL and dqPLL. Namely, for the high frequency jump step $\Delta\omega = 2\pi50$ atanPLL exhibits response times that correspond to the designed crossover frequencies ($\omega_c = 64$ rad/s in Fig. 8 (a) and (c), and $\omega_c = 114$ rad/s in Fig. 8 (b) and (d)), while dqPLL for the case of the slower crossover frequency $\omega_c = 64$ rad/s exhibits a significant decrease in the response times, caused by the nonlinear PD in dqPLL.

The experimental results are summarized in the following Table II, presented in Appendix A.

VI. Conclusion

In this paper, the novel phase-locked loop algorithm atanPLL is proposed, based on the inverse tangent atan2 function phase detection. It is shown that atanPLL enables linear phase detection, resulting in the linear PLL behaviour in all operating conditions. This is contrary to the commonly used PLL algorithms that behave nonlinearly because of the nonlinear phase detection, especially for the large phase angle and frequency jumps. In the paper, the linear behaviour of atanPLL and the nonlinear behavior of dqPLL are verified by simulation and experimental tests. It is outlined that, contrary to dqPLL that can operate consistently mainly for higher PLL crossover frequencies (i.e., for the higher PLL response speeds), novel atanPLL can operate in the whole range of the crossover frequencies, and can, also, operate linearly for large phase angle and frequency jumps. Consequently, atanPLL is more suitable in applications that require lower PLL crossover frequencies, for example, when higher filtration of noise, disturbance and harmonics is required. Finally, when compared to existing open-loop synchronization techniques that use atan function for phase angle detection, the novel technique does not use differentiation, which makes it more immune in relation to measurement noise. When compared with the most similar closed-loop solution [29], designated estimated frequency prewarping function is proposed, while the additional rotational transformations are omitted from the algorithm.

Appendix A

Table I. Rising and Settling Times for Simulation Test Responses

Item ω_c	**atanPLL** $\Delta\varphi = \pi$ **rad**	**dqPLL** $\Delta\varphi = \pi$ **rad**	**atanPLL** $\Delta\omega = 2\pi50$ **rad/s**	**dqPLL** $\Delta\omega = 2\pi50$ **rad/s**
64 rad/s	$t_{st} = 150$ ms	$t_{st} = 180$ ms	$t_r = 33$ ms	$t_r = 300$ ms
144 rad/s	$t_{st} = 80$ ms	$t_{st} = 100$ ms	$t_r = 10$ ms	$t_r = 10$ ms

TABLE II. ESTIMATED FREQUENCY VARIATIONS δ AND RISING AND SETTLING TIMES FOR EXPERIMENTAL TEST RESPONSES

Item ω_c	**atanPLL** $\Delta\varphi = \pi$ **rad**	**dqPLL** $\Delta\varphi = \pi$ **rad**	**atanPLL** $\Delta\omega = 2\pi 50$ **rad/s**	**dqPLL** $\Delta\omega = 2\pi 50$ **rad/s**
64 rad/s *Test case 1*	t_{st}=150 ms δ=1.2 rad/s	t_{st} = 190 ms δ=1.2 rad/s	t_r = 33 ms δ= 1.2 rad/s	t_r = 300 ms δ= 1.2 rad/s
144 rad/s *Test case 1*	t_{st} = 80 ms δ= 8 rad/s	t_{st} = 95 ms δ= 8 rad/s	t_r = 10 ms δ= 8 rad/s	t_r = 10 ms δ= 8 rad/s
64 rad/s *Test case 2*	t_{st} = 150 ms δ= 2 rad/s	t_{st} = 190 ms δ= 2 rad/s	t_r = 33 ms δ= 2 rad/s	t_r = 300 ms δ= 2 rad/s
144 rad/s *Test case 2*	t_{st} = 80 ms δ= 10 rad/s	t_{st} = 95 ms δ= 10 rad/s	t_r = 10 ms δ= 10 rad/s	t_r = 10 ms δ= 10 rad/s

REFERENCES

[1] S. Golestan, M. Monfared, F. D. Freijedo, J.M. Guerrero, "Dynamics assessment of advanced single-phase PLL structures," IEEE Transactions on industrial electronics, vol. 60, no. 6, pp. 2167-2177, 2013. doi:10.1109/TIE.2012.2193863

[2] R. M. Santos Filho, P. F. Seixas, P. C. Cortizo, L. A. Torres, and A. F. Souza, "Comparison of three single-phase PLL algorithms for UPS applications," IEEE Transactions on industrial electronics, vo. 55, no. 8, pp. 2923-2932, 2008. doi:10.1109/tie.2008.924205

[3] F. Baradarani, M. R. D. Zadeh, M. A. Zamani, "A Phase-angle estimation method for synchronization of grid-connected power-electronic converters," IEEE Transactions on Power Delivery, vol. 30, no. 2, pp. 827-835, 2015. doi:10.1109/TPWRD.2014.2362930

[4] M. Karimi-Ghartemani, and M. R. Iravani, "A Method for synchronization of power electronic converters in polluted and variable-frequency environments," IEEE Transactions on Power Systems, vol. 19, no. 3, pp. 1263-1270, 2004. doi:10.1109/tpwrs.2004.831280

[5] W. Li, X. Ruan, C. Bao, D. Pan, X. Wang, "Grid synchronization systems of three-phase grid-connected power converters: A complex-vector-filter perspective,"IEEE Transactions on industrial electronics, vol. 61, no. 4, pp. 1855-1870, 2014. doi:10.1109/TIE.2013.2262762

[6] Y. Han, M. Luo, X. Zhao, J. M. Guerrero, L. Xu, "Comparative performance evaluation of orthogonal-signal-generators-based single-phase PLL algorithms—a survey," IEEE Transactions on Power Electronics, vol. 31, no. 5, pp. 3932-3944, 2016. doi:10.1109/TPEL.2015.2466631

[7] A. Luna, J. Rocabert, J. I. Candela, J. R. Hermoso, R. Teodorescu, F. Blaabjerg P. Rodriguez, "Grid voltage synchronization for distributed generation systems under grid fault conditions," IEEE Transactions on Industry Applications, vol. 51, no. 4, pp. 3414-3425, 2015. doi:10.1109/tia.2015.2391436

[8] A. Timbus, M. Liserre, R. Teodorescu, F. Blaabjerg, "Synchronization Methods for Three Phase Distributed Power Generation Systems-an Overview and Evaluation," in Power Electronics Specialists Conference, PESC'05. IEEE 36th, 2005. doi:10.1109/pesc.2005.1581980

[9] F. Blaabjerg, R. Teodorescu, M. Liserre, A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," IEEE Transactions on industrial electronics, vol. 53, no. 5, pp. 1398-1409, 2006. doi:10.1109/tie.2006.881997

[10] M. Comanescu, L. Xu, "An improved flux observer based on PLL frequency estimator for sensorless vector control of induction motors," Industrial Electronics, IEEE Transactions on, vol. 53, no. 1, pp. 50-56, 2006. doi:10.1109/tie.2005.862317

[11] V. Kaura, V. Blasko, "Operation of a phase locked loop system under distorted utility conditions," IEEE Transactions on Industry Applications, vol. 33, no. 1, pp. 58-63, 1997. doi:10.1109/28.567077

[12] P. Rodriguez, A. Luna, M. Ciobotaru, R. Teodorescu, F. Blaabjerg, "Advanced grid synchronization system for power converters under unbalanced and distorted operating conditions," IEEE Industrial Electronics, IECON 2006-32nd Annual Conference on, 2006. doi:10.1109/iecon.2006.347807

[13] A. V. Timbus, R. Teodorescu, F. Blaabjerg, M. Liserre, P. Rodriguez, "PLL algorithm for power generation systems robust to grid voltage faults," in Proc. of PESC, 2006. doi:10.1109/PESC.2006.1711963

[14] L. Liu, H. Li, Z. Wu, Y. Zhou, "A cascaded photovoltaic system integrating segmented energy storages with self-regulating power allocation control and wide range reactive power compensation," IEEE Transactions on Power Electronics, vol. 26, no. 12, pp. 3545-3559, 2011. doi:10.1109/tpel.2011.2168544

[15] M. Padua, S. Deckmann, G. Sperandio, F. Marafao, D. Colon, "Comparative analysis of synchronization algorithms based on PLL, RDFT and Kalman filter," in Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on, 2007. doi:10.1109/isie.2007.4374728

[16] G. H. Jung, G. C. Cho, S. W. Hong, G. H. Cho, "Dsp based control of high power static VAr compensator using novel vector product phase locked loop," in Power Electronics Specialists Conference, 1996. PESC'96 Record., 27th Annual IEEE, 1996. doi:10.1109/pesc.1996.548587

[17] L. Zheng, H. Geng, G. Yang, "Fast and robust phase estimation algorithm for heavily distorted grid conditions," IEEE Transactions on industrial electronics, vol. 63, no. 11, pp. 6845-6855, 2016. doi:10.1109/TIE.2016.2585078

[18] S. Golestan, M. Ramezani, J. M. Guerrero, F. D. Freijedo, M. Monfared, "Moving average filter based phase-locked loops: Performance analysis and design guidelines," IEEE Transactions on Power Electronics, vol. 29, no. 6, pp. 2750-2763, 2014. doi:10.1109/TPEL.2013.2273461

[19] S. Chandrasekaran, K. Ragavan, "Adaptive sampling period adjusted sliding DFT for synchronous reference frame PLL," in Power Electronics, Drives and Energy Systems (PEDES), 2014 IEEE International Conference on, 2014. doi:10.1109/pedes.2014.7041974

[20] F. Cupertino, E. Lavopa, P. Zanchetta, M. Sumner, L. Salvatore, "Running DFT-based PLL algorithm for frequency, phase, and amplitude tracking in aircraft electrical systems," IEEE Transactions on industrial electronics, vol. 58, no. 3, pp. 1027-1035, 2011. doi: 10.1109/tie.2010.2048293

[21] N. Guerrero-Rodríguez, A. B. Rey-Boué, E. Bueno, O. Ortiz, E. Reyes-Archundia, "Synchronization algorithms for grid-connected renewable systems: Overview, tests and comparative analysis," Renewable and Sustainable Energy Reviews, 2016. doi:10.1016/j.rser.2016.11.038

[22] Y. F. Wang, Y. W. Li, "Grid synchronization PLL based on cascaded delayed signal cancellation," IEEE Transactions on Power Electronics, vol. 26, no. 7, pp. 1987-1997, 2011. doi:10.1109/TPEL.2010.2099669

[23] S. Golestan, J. M. Guerrero, J. C. Vasquez, "Three-phase PLLs: a review of recent advances," IEEE Transactions on Power Electronics, vol. 32, no. 3, pp. 1894-1907, 2017. doi:10.1109/TPEL.2016.2565642

[24] R. Teodorescu, M. Liserre, P. Rodriguez, "Grid converters for photovoltaic and wind power systems," John Wiley & Sons, 2011. doi:10.1109/mie.2011.941116

[25] S. Golestan, A. Vidal, A. G. Yepes, J. M. Guerrero, J. C. Vasquez, J. Doval-Gandoy, "A true open-loop synchronization technique," *IEEE Transactions on Industrial Informatics*, vol. 12, no. 3, pp. 1093-1103, 2016. doi: 10.1109/tii.2016.2550017

[26] F. Xiao, L. Dong, L. Li, X. Liao, "A novel open-loop frequency estimation method for single-phase grid synchronization under distorted conditions," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 3, pp. 1287-1297, 2017. doi:10.1109/JESTPE.2017.2685620

[27] A. K. Verma, R. K. Jarial, P. Roncero-Sanchez, M. R. Ungarala, J. M. Guerrero, "An improved hybrid pre-filtered open-loop algorithm for three-phase grid synchronization," IEEE Transactions on Industrial Electronics 2020. doi:10.1109/TIE.2020.2975470

[28] Z. Ali, N. Christofides, L. Hadjidemetriou, E. Kyriakides, Y. Yang, F. Blaabjerg, "Three-phase phase-locked loop synchronization algorithms for grid-connected renewable energy systems: A review," Renewable and Sustainable Energy Reviews, vol. 90, pp. 434-452, 2018. doi:10.1016/j.rser.2018.03.086

[29] S. Golestan, F. D. Freijedo, A. Vidal, J. M. Guerrero, J. Doval-Gandoy, "A quasi-type-1 phase-locked loop structure," IEEE Transactions on Power Electronics, vol. 29, no. 12, pp. 6264-6270, 2014. doi: 10.1109/TPEL.2014.2329917

[30] S. Preitl, R.-E. Precup, "An extension of tuning relations after symmetrical optimum method for PI and PID controllers," Automatica, vol. 35, no. 10, pp. 1731-1736, Oct. 1999. doi:10.1016/S0005-1098(99)00091-6

[31] T. Haidegger, K. Levente , R.-E. Precup, S. Preitl, B. Benyó, Z. Benyó, "Cascade control for telerobotic systems serving space medicine," IFAC Proceedings, vol. 44, no. 1, 2011, pp. 3759-3764. doi: 10.3182/20110828-6-IT-1002.02482